Sitronix

ST7565P

65 x 132 Dot Matrix LCD Controller/Driver

INTRODUCTION

ST7565P is a single-chip dot matrix LCD driver which incorporates LCD controller and common/segment drivers. ST7565P can be connected directly to a microprocessor with 8-bit parallel interface or 4-line serial interface (SPI-4). Display data sent from MPU is stored in the internal Display Data RAM (DDRAM) of 65x132 bits. The display data bits which are stored in DDRAM are directly related to the pixels of LCD panel. ST7565P contains 132 segment-outputs, 64 common-outputs and 1 icon-common-output. With built-in oscillation circuit and low power consumption power circuit, ST7565P generates LCD driving signal without external clock or power, so that it is possible to make a display system with the minimal power consumption. The horizontal display area can be extended by master and slave functionality.

FEATURES

Single-chip LCD Controller & Driver

On-chip Display Data RAM (DDRAM)

- Capacity: 65x132=8580 bits
- Directly display RAM pattern from DDRAM

Selectable Display Duty (by SEL3 & SEL2 & SEL1)

- 1/65 duty : 65 common x 132 segment
- 1/55 duty : 55 common x 132 segment
- 1/53 duty : 53 common x 132 segment
- 1/49 duty : 49 common x 132 segment
- 1/33 duty : 33 common x 132 segment

Microprocessor Interface

- Bidirectional 8-bit parallel interface supports: 8080-series and 6800-series MPU
- Serial interface (SPI-4) is also supported (write only)

Abundant Functions

- Display ON/OFF, Normal/Reverse Display Mode, Set Display Start Line, Read IC Status, Set all Display Points ON, Set LCD Bias, Electronic Volume Control, Read-modify-Write, Select Segment Driver Direction, Power Saving Mode, Select Common Driver Direction, Select Voltage Regulator Resistor Ratio (for V0).

External Hardware Reset Pin (RSTB)

Built-in Oscillation Circuit

- No external component required
- The external clock is also supported.

Low Power Consumption Analog Circuit

- Built-in Voltage Booster (x2~x6)
- High-accuracy Voltage Regulator for LCD Vop: (Thermal Gradient: -0.05%/℃)
- Voltage Follower for LCD Bias Voltage

Wide Operation Voltage Range

- VDD1-VSS=1.8V~3.3V (Typical)
- VDD2-VSS=2.4V~3.3V (Typical)

Temperature Range: -30~80℃

Package Type: COG & TCP

ST7565P	6800 , 8080 , 4-Line	

ST7565P COG OUTLINE

Chip Size: 9336 X 1000

Bump Height: 9 (for G-1)

Bump Pitch: 58 (Min.) **Unit: um**

Part Number	Chip Thickness
ST7565P	635
Bump Size	
PAD No.	Size
1~12, 103~114, 129~276	40 x 90
13~102	56 x 60
115, 290	90 x 25.5
116~128, 277~289	90 x 40
*** Refer to section "PAD CENTER COORDINATES" for ITO layout.**	

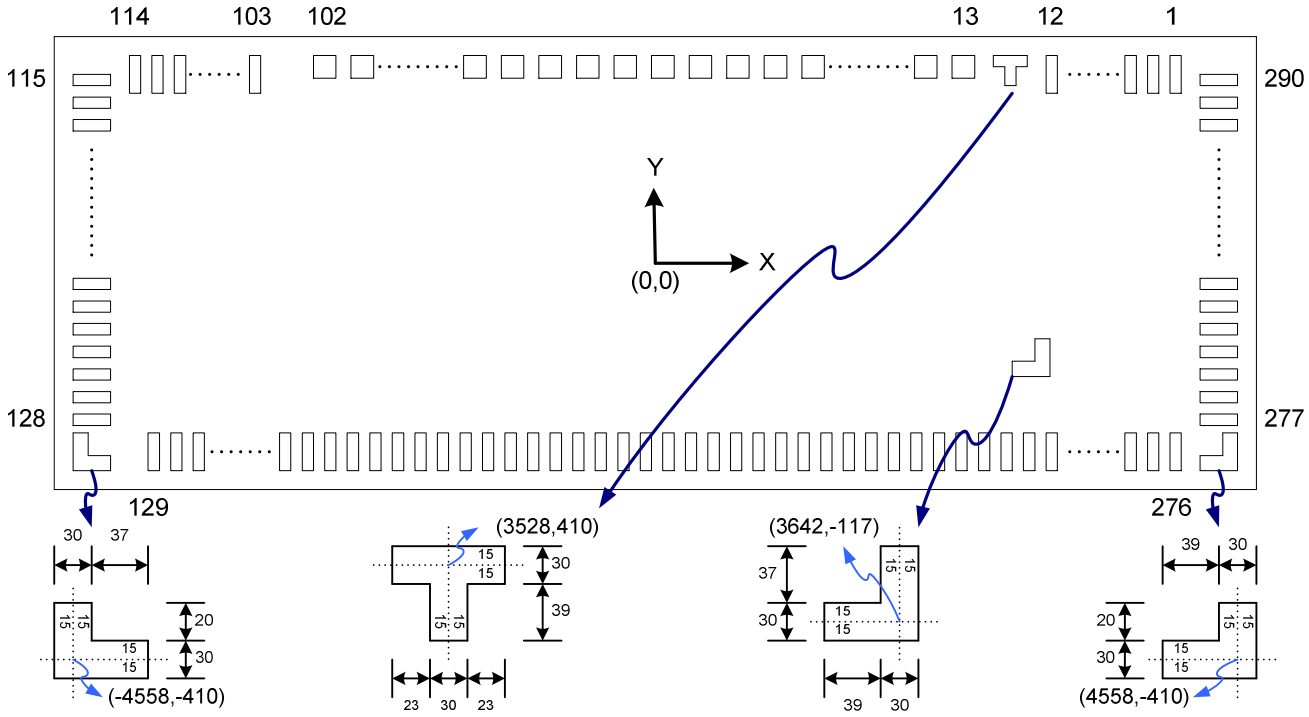


Fig 1. Chip Outline

PAD CENTER COORDINATES

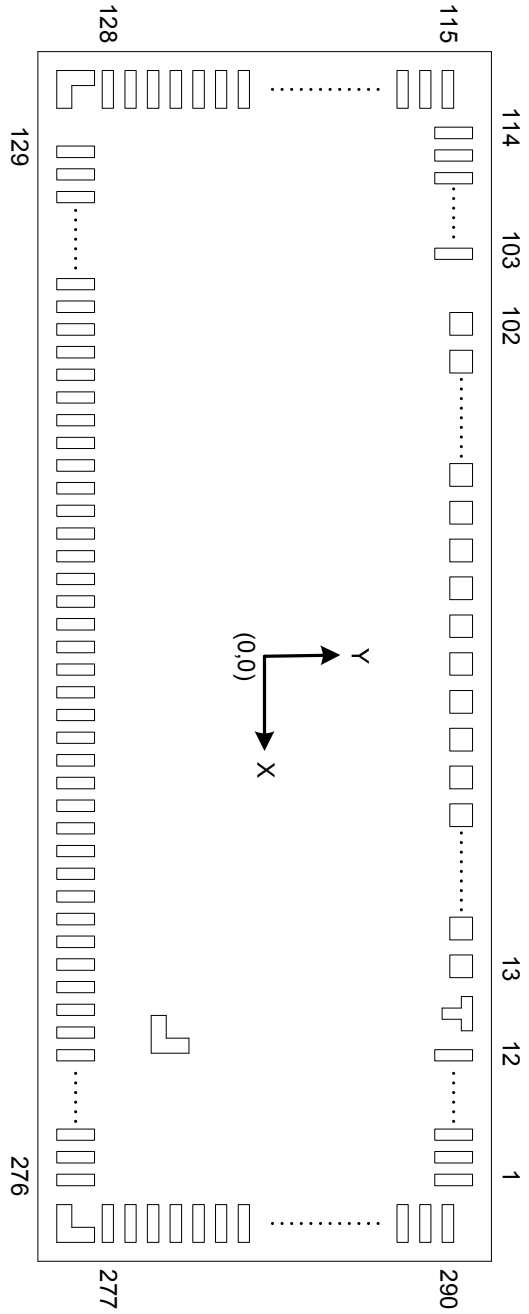


Fig 2. PAD Location

65 Duty

PAD NO.	PIN Name	X	Y
1	COM[53]	4241	374
2	COM[54]	4183	374
3	COM[55]	4125	374
4	COM[56]	4067	374
5	COM[57]	4009	374
6	COM[58]	3951	374
7	COM[59]	3893	374
8	COM[60]	3835	374
9	COM[61]	3777	374
10	COM[62]	3719	374
11	COM[63]	3661	374
12	COMS1	3603	374
13	FRS	3443	389
14	FR	3369	389
15	CL	3295	389
16	DOFB	3221	389
17	VSS	3147	389
18	CS1B	3073	389
19	CS2	2999	389
20	VDD	2925	389
21	RSTB	2851	389
22	A0	2777	389
23	VSS	2703	389
24	RWR	2629	389
25	ERD	2555	389
26	VDD	2481	389
27	D0	2407	389
28	D1	2333	389
29	D2	2259	389
30	D3	2185	389
31	D4	2111	389
32	D5	2037	389
33	D6	1963	389
34	D7	1889	389
35	VDD	1815	389
36	VDD2	1741	389
37	VDD2	1667	389
38	VSS	1593	389
39	VSS	1519	389
40	VSS	1445	389

PAD NO.	PIN Name	X	Y
41	VSS	1371	389
42	VOUT	1297	389
43	VOUT	1223	389
44	CAP5P	1149	389
45	CAP5P	1075	389
46	CAP1N	1001	389
47	CAP1N	927	389
48	CAP3P	853	389
49	CAP3P	779	389
50	CAP1N	705	389
51	CAP1N	631	389
52	CAP1P	557	389
53	CAP1P	483	389
54	CAP2P	409	389
55	CAP2P	335	389
56	CAP2N	261	389
57	CAP2N	187	389
58	CAP4P	113	389
59	CAP4P	39	389
60	VSS	-35	389
61	VSS	-109	389
62	VRS	-183	389
63	VRS	-257	389
64	VDD2	-331	389
65	VDD	-405	389
66	V4	-479	389
67	V4	-553	389
68	V3	-627	389
69	V3	-701	389
70	V2	-775	389
71	V2	-849	389
72	V1	-923	389
73	V1	-997	389
74	V0	-1071	389
75	V0	-1145	389
76	VR	-1219	389
77	VR	-1293	389
78	VDD	-1367	389
79	VDD2	-1441	389
80	TEST0	-1515	389

PAD NO.	PIN Name	X	Y
81	TEST1	-1589	389
82	TEST2	-1663	389
83	TEST3	-1737	389
84	TEST4	-1811	389
85	TEST5	-1885	389
86	VDD	-1959	389
87	M/S	-2033	389
88	CLS	-2107	389
89	VSS	-2181	389
90	C86	-2255	389
91	P/S	-2329	389
92	VDD	-2403	389
93	/HPM	-2477	389
94	VSS	-2551	389
95	IRS	-2625	389
96	VDD	-2699	389
97	SEL1	-2773	389
98	VSS	-2847	389
99	SEL2	-2921	389
100	VDD	-2995	389
101	SEL3	-3069	389
102	VSS	-3143	389
103	COM[31]	-3606	374
104	COM[30]	-3664	374
105	COM[29]	-3722	374
106	COM[28]	-3780	374
107	COM[27]	-3838	374
108	COM[26]	-3896	374
109	COM[25]	-3954	374
110	COM[24]	-4012	374
111	COM[23]	-4070	374
112	COM[22]	-4128	374
113	COM[21]	-4186	374
114	COM[20]	-4244	374
115	Reserved	-4542	404
116	COM[19]	-4542	351
117	COM[18]	-4542	293
118	COM[17]	-4542	235
119	COM[16]	-4542	177
120	COM[15]	-4542	119

PAD NO.	PIN Name	X	Y
121	COM[14]	-4542	61
122	COM[13]	-4542	3
123	COM[12]	-4542	-55
124	COM[11]	-4542	-113
125	COM[10]	-4542	-171
126	COM[9]	-4542	-229
127	COM[8]	-4542	-287
128	COM[7]	-4542	-345
129	COM[6]	-4267	-374
130	COM[5]	-4209	-374
131	COM[4]	-4151	-374
132	COM[3]	-4093	-374
133	COM[2]	-4035	-374
134	COM[1]	-3977	-374
135	COM[0]	-3919	-374
136	COMS2	-3861	-374
137	SEG[0]	-3803	-374
138	SEG[1]	-3745	-374
139	SEG[2]	-3687	-374
140	SEG[3]	-3629	-374
141	SEG[4]	-3571	-374
142	SEG[5]	-3513	-374
143	SEG[6]	-3455	-374
144	SEG[7]	-3397	-374
145	SEG[8]	-3339	-374
146	SEG[9]	-3281	-374
147	SEG[10]	-3223	-374
148	SEG[11]	-3165	-374
149	SEG[12]	-3107	-374
150	SEG[13]	-3049	-374
151	SEG[14]	-2991	-374
152	SEG[15]	-2933	-374
153	SEG[16]	-2875	-374
154	SEG[17]	-2817	-374
155	SEG[18]	-2759	-374
156	SEG[19]	-2701	-374
157	SEG[20]	-2643	-374
158	SEG[21]	-2585	-374
159	SEG[22]	-2527	-374
160	SEG[23]	-2469	-374

PAD NO.	PIN Name	X	Y
161	SEG[24]	-2411	-374
162	SEG[25]	-2353	-374
163	SEG[26]	-2295	-374
164	SEG[27]	-2237	-374
165	SEG[28]	-2179	-374
166	SEG[29]	-2121	-374
167	SEG[30]	-2063	-374
168	SEG[31]	-2005	-374
169	SEG[32]	-1947	-374
170	SEG[33]	-1889	-374
171	SEG[34]	-1831	-374
172	SEG[35]	-1773	-374
173	SEG[36]	-1715	-374
174	SEG[37]	-1657	-374
175	SEG[38]	-1599	-374
176	SEG[39]	-1541	-374
177	SEG[40]	-1483	-374
178	SEG[41]	-1425	-374
179	SEG[42]	-1367	-374
180	SEG[43]	-1309	-374
181	SEG[44]	-1251	-374
182	SEG[45]	-1193	-374
183	SEG[46]	-1135	-374
184	SEG[47]	-1077	-374
185	SEG[48]	-1019	-374
186	SEG[49]	-961	-374
187	SEG[50]	-903	-374
188	SEG[51]	-845	-374
189	SEG[52]	-787	-374
190	SEG[53]	-729	-374
191	SEG[54]	-671	-374
192	SEG[55]	-613	-374
193	SEG[56]	-555	-374
194	SEG[57]	-497	-374
195	SEG[58]	-439	-374
196	SEG[59]	-381	-374
197	SEG[60]	-323	-374
198	SEG[61]	-265	-374
199	SEG[62]	-207	-374
200	SEG[63]	-149	-374

PAD NO.	PIN Name	X	Y
201	SEG[64]	-91	-374
202	SEG[65]	-33	-374
203	SEG[66]	25	-374
204	SEG[67]	83	-374
205	SEG[68]	141	-374
206	SEG[69]	199	-374
207	SEG[70]	257	-374
208	SEG[71]	315	-374
209	SEG[72]	373	-374
210	SEG[73]	431	-374
211	SEG[74]	489	-374
212	SEG[75]	547	-374
213	SEG[76]	605	-374
214	SEG[77]	663	-374
215	SEG[78]	721	-374
216	SEG[79]	779	-374
217	SEG[80]	837	-374
218	SEG[81]	895	-374
219	SEG[82]	953	-374
220	SEG[83]	1011	-374
221	SEG[84]	1069	-374
222	SEG[85]	1127	-374
223	SEG[86]	1185	-374
224	SEG[87]	1243	-374
225	SEG[88]	1301	-374
226	SEG[89]	1359	-374
227	SEG[90]	1417	-374
228	SEG[91]	1475	-374
229	SEG[92]	1533	-374
230	SEG[93]	1591	-374
231	SEG[94]	1649	-374
232	SEG[95]	1707	-374
233	SEG[96]	1765	-374
234	SEG[97]	1823	-374
235	SEG[98]	1881	-374
236	SEG[99]	1939	-374
237	SEG[100]	1997	-374
238	SEG[101]	2055	-374
239	SEG[102]	2113	-374
240	SEG[103]	2171	-374

PAD NO.	PIN Name	X	Y
241	SEG[104]	2229	-374
242	SEG[105]	2287	-374
243	SEG[106]	2345	-374
244	SEG[107]	2403	-374
245	SEG[108]	2461	-374
246	SEG[109]	2519	-374
247	SEG[110]	2577	-374
248	SEG[111]	2635	-374
249	SEG[112]	2693	-374
250	SEG[113]	2751	-374
251	SEG[114]	2809	-374
252	SEG[115]	2867	-374
253	SEG[116]	2925	-374
254	SEG[117]	2983	-374
255	SEG[118]	3041	-374
256	SEG[119]	3099	-374
257	SEG[120]	3157	-374
258	SEG[121]	3215	-374
259	SEG[122]	3273	-374
260	SEG[123]	3331	-374
261	SEG[124]	3389	-374
262	SEG[125]	3447	-374
263	SEG[126]	3505	-374
264	SEG[127]	3563	-374
265	SEG[128]	3621	-374
266	SEG[129]	3679	-374
267	SEG[130]	3737	-374
268	SEG[131]	3795	-374
269	COM[32]	3853	-374
270	COM[33]	3911	-374
271	COM[34]	3969	-374
272	COM[35]	4027	-374
273	COM[36]	4085	-374
274	COM[37]	4143	-374
275	COM[38]	4201	-374
276	COM[39]	4259	-374
277	COM[40]	4542	-345
278	COM[41]	4542	-287
279	COM[42]	4542	-229
280	COM[43]	4542	-171

PAD NO.	PIN Name	X	Y
281	COM[44]	4542	-113
282	COM[45]	4542	-55
283	COM[46]	4542	3
284	COM[47]	4542	61
285	COM[48]	4542	119
286	COM[49]	4542	177
287	COM[50]	4542	235
288	COM[51]	4542	293
289	COM[52]	4542	351
290	Reserved	4542	404

Note:

1. Unit: um
2. This is the default PAD Center Coordinate Table with 1/65 Duty. Other duty output mapping can be found in Section FUNCTION DESCRIPTION and Fig 9.
3. Tolerance: +/- 0.05 um.
4. **The definition of pin name is in full duty (1/65 Duty).**
5. **The definition of output pin name in different duty (1/55 Duty, 1/53 Duty, 1/49 Duty and 1/33 Duty) please refers Fig 9.**

BLOCK DIAGRAM

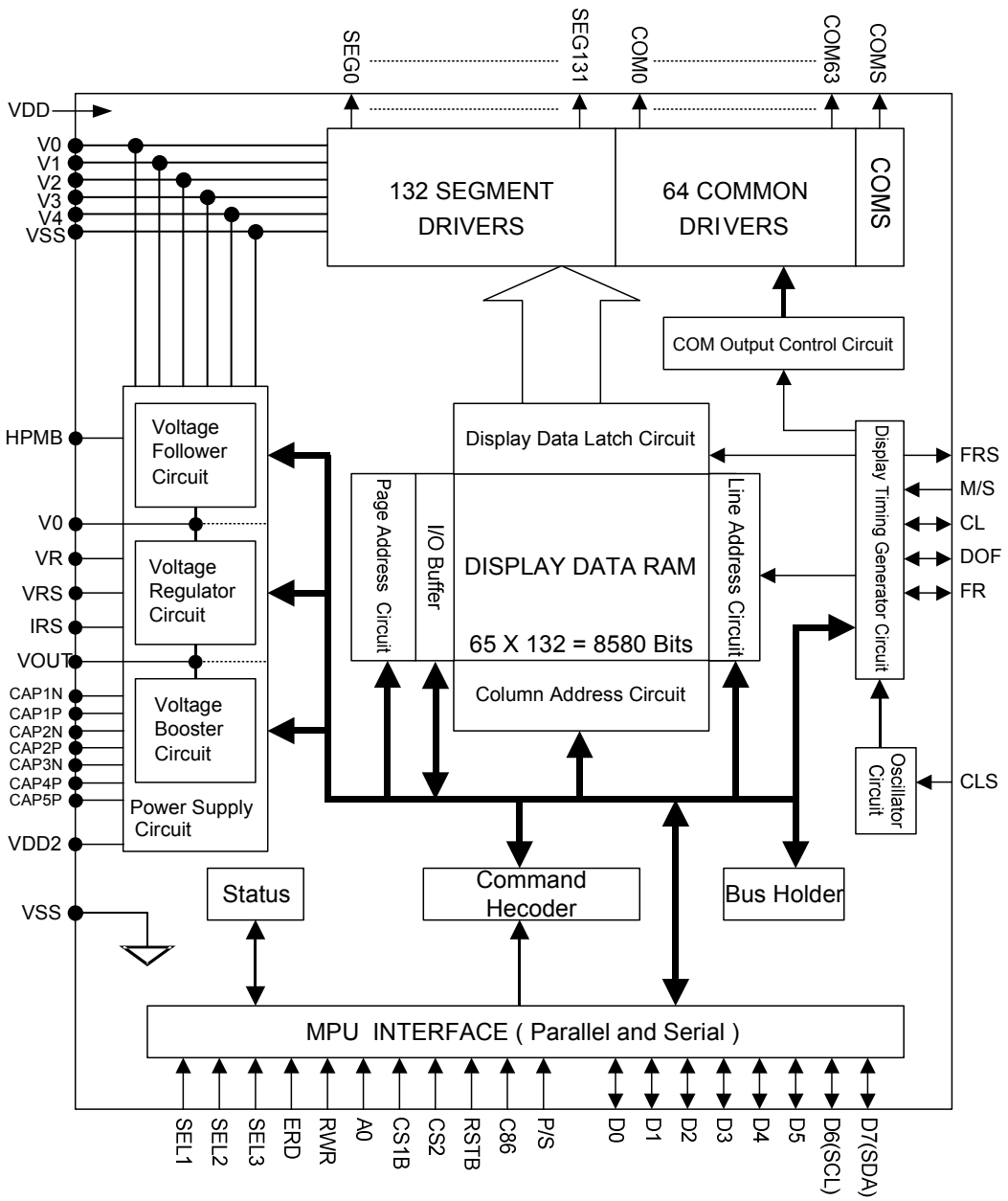


Fig 3. Block Diagram

PIN DESCRIPTION

LCD Driver Output Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>SEG0 to SEG131</td><td>O</td><td>LCD segment driver outputs.
The display data and the frame control the output voltage.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">Frame</th><th colspan="2">Segment Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td rowspan="2">H</td><td>+</td><td>V0</td><td>V2</td></tr>
<tr><td>-</td><td>VSS</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>+</td><td>V2</td><td>V0</td></tr>
<tr><td>-</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td>VSS</td><td>VSS</td></tr>
</table></td><td>132</td></tr>
<tr><td>COM0 to COM63</td><td>O</td><td>LCD common driver outputs.
The internal scanning signal and the frame control the output voltage.
<table>
<tr><th rowspan="2">Scan signal</th><th rowspan="2">Frame</th><th colspan="2">Common Driver Output Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td rowspan="2">H</td><td>+</td><td colspan="2">VSS</td></tr>
<tr><td>-</td><td colspan="2">V0</td></tr>
<tr><td rowspan="2">L</td><td>+</td><td colspan="2">V1</td></tr>
<tr><td>-</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Display OFF, Power Save</td><td colspan="2">VSS</td></tr>
</table></td><td>64</td></tr>
<tr><td>COMS1, COMS2
(COMS)</td><td>O</td><td>LCD common driver outputs for icons.
The output signals of these two pins are the same.
When icon feature is not used, these pins should be left open.</td><td>2</td></tr>
</table>

Microprocessor Interface Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>RSTB</td><td>I</td><td>Hardware reset input pin. When RSTB is “L”, internal initialization is executed and the internal registers will be initialized.</td><td>1</td></tr>
<tr><td>CS1B
CB2</td><td>I</td><td>Chip select input pin. Interface access is enabled when CS1B is “L” and CB2 is “H”. When chip is on-active (CS1B=“H” or CS2=”L”), D[7:0] pins are high impedance.</td><td>1
1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the access is related to data or command.
A0=“H”: Indicates that signals on D[7:0] are display data.
A0=“L”: Indicates that signals on D[7:0] are command.</td><td>1</td></tr>
<tr><td>RWR</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”,
<table>
<tr><th>C86</th><th>MPU Type</th><th>RWR</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>R/W</td><td>Read/Write control input pin.
R/W=“H”: read.
R/W=“L”: write.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/WR</td><td>Write enable input pin.
Signals on D[7:0] will be latched at the rising edge of /WR signal.</td></tr>
</table>
RWR is not used in serial interface and should fix to “H” by VDD.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>ERD</td><td>I</td><td>Read/Write execution control pin. When PSB is “H”,
<table>
<tr><th>C86</th><th>MPU Type</th><th>ERD</th><th>Description</th></tr>
<tr><td>H</td><td>6800 series</td><td>E</td><td>Read/Write control input pin.
R/W=”H“: When E is “H”, D[7:0] are in output mode.
R/W=”L“: Signals on D[7:0] are latched at the falling edge of E signal.</td></tr>
<tr><td>L</td><td>8080 series</td><td>/RD</td><td>Read enable input pin.
When /RD is “L”, D[7:0] are in output mode.</td></tr>
</table>
ERD is not used in serial interface and should fix to “H” by VDD.</td><td>1</td></tr>
<tr><td rowspan="2">D[7:0]</td><td>I/O</td><td>When using 8-bit parallel interface: (6800 or 8080 mode)
8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor.
When CS1B and CS2 are non-active (CS1B=“H” & CS2=”L”), D[7:0] pins are high impedance.</td><td rowspan="2">8</td></tr>
<tr><td>I</td><td>When using serial interface: 4-LINE
D7=SDA: Serial data input.
D6=SCL: Serial clock input.
D[5:0] are not used and should connect to “H” by VDD.
When CS1B and CS2 are non-active (CS1B=“H” & CS2=”L”), D[7:0] pins are high impedance.</td></tr>
</table>

Note:

1. After VDD is turned ON, any MPU interface pins cannot be left floating.

Configuration Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>PSB</td><td>I</td><td>PSB selects the interface type: Serial or Parallel.</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>C86 selects the microprocessor type in parallel interface mode.
<table>
<tr><th>PSB</th><th>C86</th><th>Selected Interface</th></tr>
<tr><td>“H”</td><td>“H”</td><td>Parallel 6800 Series MPU Interface</td></tr>
<tr><td>“H”</td><td>“L”</td><td>Parallel 8080 Series MPU Interface</td></tr>
<tr><td>“L”</td><td>“X”</td><td>Serial 4-Line SPI Interface</td></tr>
</table>
Please refer to “APPLICATION NOTES” and “Microprocessor Interface” (Section 6) for detailed connection of the selected interface.</td><td>1</td></tr>
<tr><td>SEL[3:1]</td><td>I</td><td>These pins select the display duty and bias of ST7565P.
<table>
<tr><th>SEL3</th><th>SEL2</th><th>SEL1</th><th>Duty</th><th>Bias</th></tr>
<tr><td>“L”</td><td>“L”</td><td>“L”</td><td>1/65</td><td>1/9 or 1/7</td></tr>
<tr><td>“L”</td><td>“L”</td><td>“H”</td><td>1/49</td><td>1/8 or 1/6</td></tr>
<tr><td>“L”</td><td>“H”</td><td>“L”</td><td>1/33</td><td>1/6 or 1/5</td></tr>
<tr><td>“L”</td><td>“H”</td><td>“H”</td><td>1/55</td><td>1/8 or 1/6</td></tr>
<tr><td>“H”</td><td>“L”</td><td>“L”</td><td>1/53</td><td>1/8 or 1/6</td></tr>
<tr><td>“H”</td><td>-</td><td>0</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note:
1. The detailed definition of output pin name can be found in Fig 9.</td><td>3</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>CLS</td><td>I</td><td>This pin selects built-in OSC circuit is enable or disable.
CLS=”H”: built-in OSC circuit is enabled.
CLS=”L”: built-in OSC circuit is disabled.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>This pin selects built-in resistor for V0 adjustment is enable or disable.
IRS=H”: built-in resistor is enabled.
IRS=”L”: built-in resistor is disabled.</td><td>1</td></tr>
<tr><td>HPMB</td><td>I</td><td>This pin is used to select power supply mode.
HPMB=”H”: normal mode.
HPMB=”L”: high power mode (suggested).</td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>This pin is used for select master or slave operation.
M/S=”H”: master mode
M/S=”L”: slave mode
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator Circuit</th><th>Power Supply Circuit</th><th>CL</th><th>FR</th><th>DOF</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>ON</td><td>ON</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>“L”</td><td>OFF</td><td>ON</td><td>Input</td><td>Output</td><td>Output</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>OFF</td><td>OFF</td><td>Input</td><td>Input</td><td>Input</td></tr>
<tr><td>“L”</td><td>OFF</td><td>OFF</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table></td><td>1</td></tr>
</table>

Power System Pins

Pin Name	Type	Description	No. of Pins
VDD	**Power**	Digital power. If VDD=VDD2, connect to VDD2 externally.	**13**
VDD2	**Power**	Analog power. If VDD=VDD2, connect to VDD externally.	**10**
VSS	**Power**	Ground of chip.	**2**
VRS	**Power**	This pin is output internal VREG power for built-in LCD power circuit.	**2**
VOUT	**Power**	DC-DC voltage converter for LCD driver circuit. Connect a capacitor between VOUT and VSS.	**2**
CAP1P	**Power**	DC-DC voltage converter for LCD driver circuit. If using built-in voltage booster circuit, the application circuit please refers to section of Liquid Crystal Driver Power Circuit.	**4**
CAP1N			**2**
CAP2P			**2**
CAP2N			**2**
CAP3P			**2**
CAP4P			**2**
CAP5P			**2**
V0	**Power**	The power supply pins for LCD. Insure the voltage levels of VOUT, V0, V1, V2, V3 and V4 always match below relation: VOUT > V0 > V1 > V2 > V3 > V4 > VSS	**2**
V1			**2**
V2			**2**
V3			**2**
V4			**2**
VR	**Power**	If using external resistance for V0 voltage regulator, this pin is provided to connect external resistor for voltage divide.	**2**

Signal Pins

<table>
<tr><th>Pin Name</th><th>Type</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td>CL</td><td>I/O</td><td>This pin is clock input terminal.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td rowspan="2">“H”</td><td>“H”</td><td>Output</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
<tr><td rowspan="2">“L”</td><td>“H”</td><td>Input</td></tr>
<tr><td>“L”</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>DOFB</td><td>I/O</td><td>This pin is used to control slaver display blanking.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>This pin is the liquid crystal alternating signal.</td><td>1</td></tr>
</table>

Test Pins

Pin Name	Type	Description	No. of Pins
TEST[5:0]	**T**	Do NOT use. Reserved for testing. TEST[5:0] must be floating.	**6**
FRS	**T**	Do Not use. Reserved for testing.	**1**

Recommend ITO Resistance

Pin Name	ITO Resistance
TEST[5:0], VRS	Floating
C86, PSB, HPMB, SEL[3:1], CLS, IRS, M/S	No Limitation
VDD, VDD2, VSS, VOUT, VR	< 100Ω
V0, V1, V2, V3, V4, CAP1P, CAP1N, CAP2P, CAP2N, CAP3P, CAP4P, CAP5P	< 300Ω
CS1B, CS2, ERD, RWR, A0, D[7:0], FR, DOFB, CL	< 1KΩ
RSTB	< 10KΩ

Note:

1. To prevent the ESD pulse resetting the internal register, applications should increase the resistance of RSTB signal (add a series resistor or increase ITO resistance). The value is different from modules.
2. The option setting to be “H” should connect to VDD.
3. The option setting to be “L” should connect to VSS.

FUNCTION DESCRIPTION

Microprocessor Interface

Chip Select Input

CS1B and CS2 pins are used for chip selection. When CS1B="L" and CS2="H", the microprocessor interface is enabled and ST7565P can interface with an MPU. When CS1B="H" or CS2="L", the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 4-Line serial interface, the internal shift register and serial counter are reset when CS1B="H" or CS2="L".

MCU Interface Selection

The interface selection is controlled by C86 and PSB pins. The selection for parallel or serial interface is shown in Table 1.

Table 1. Parallel/Serial Interface Mode

PSB	C86	CS1B	CS2	A0	ERD	RWR	D[7:0]	MPU Interface
"H"	"H"	CS1B	CS2	A0	E	R/W	D[7:0]	6800-series parallel interface
"H"	"L"				/RD	/WR		8080-series parallel interface
"L"	"X"				-	-	Refer to serial interface.	4-Line SPI interface

* The un-used pins are marked as "-" and should be fixed to "H" by VDD.

Parallel Interface

When PSB= "H", the 8-bit bi-directional parallel interface is enabled and the type of MPU is selected by "C86" pin as shown in Table 2. The data transfer type is determined by signals on A0, ERD and RWR as shown in Table 3.

Table 2. Microprocessor Selection for Parallel Interface

PSB	C86	CS1B	CS2	A0	ERD	RWR	D[7:0]	MPU Interface
"H"	"H"	CS1B	CS2	A0	E	R/W	D[7:0]	6800-series parallel interface
	"L"				/RD	/WR		8080-series parallel interface

Table 3. Parallel Data Transfer Type

Common Pins			6800-Series		8080-Series		Description
CS1B	CS2	A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
"L"	"H"	"H"	"H"	"H"	"L"	"H"	Display data read out
		"H"	"H"	"L"	"H"	"L"	Display data write
		"L"	"H"	"H"	"L"	"H"	Internal status read
		"L"	"H"	"L"	"H"	"L"	Writes to internal register (instruction)

Setting Serial Interface

Serial Mode	PSB	C86	CS1B	CS2	A0	ERD	RWR	D7	D6	D[5:0]
4-Line SPI interface	"L"	X	CS1B	CS2	A0	-	-	SDA	SCLK	-

* The un-used pins are marked as "-" and should be fixed to "H" by VDD.

* C86 is marked as "X" and can be fixed to "H" or "L".

Note:

1. The option setting to be "H" should connect to VDD.
2. The option setting to be "L" should connect to VSS.

4-line SPI interface (PSB="L", C86="H" or "L")

When ST7565P is active (CS1B="L" and CS2="H"), serial data (SDA) and serial clock (SCLK) inputs are enabled. When ST7565P is not active (CS1B="H" or CS2="L"), the internal 8-bit shift register and 3-bit counter are reset. Serial data on SDA is latched at the rising edge of serial clock on SCLK. After the 8th serial clock, the serial data will be processed to be 8-bit parallel data. The address selection pin (A0), which is latched at the 8th clock, indicates the 8-bit parallel data is display data or instruction. The 8-bit parallel data will be display data when A0 is "H" and will be instruction when A0 is "L". The read feature is not available in this mode. The DDRAM column address pointer will be increased by one automatically after each byte of DDRAM access. Please note that the SCLK signal quality is very important and external noise maybe causes unexpected data/instruction latch.

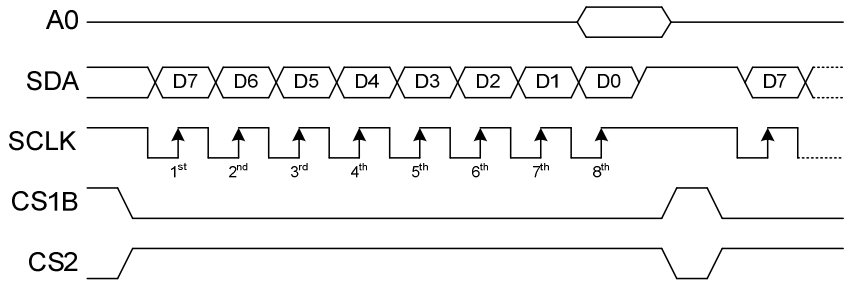


Fig 4. 4-Line SPI Access

Note:

- Some MPU will set the interface to be Hi-Z (high impedance) mode when power saving mode or after hardware reset. This is not allowed when the VDD of ST7565P is turned ON. Because the floating input (especially for those control pins such as CS1B, CS2, RSTB, RWR or ERD…) maybe cause abnormal latch and cause abnormal display.

Data Transfer

ST7565P uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM as shown in Fig 5. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle as shown in Fig 6. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

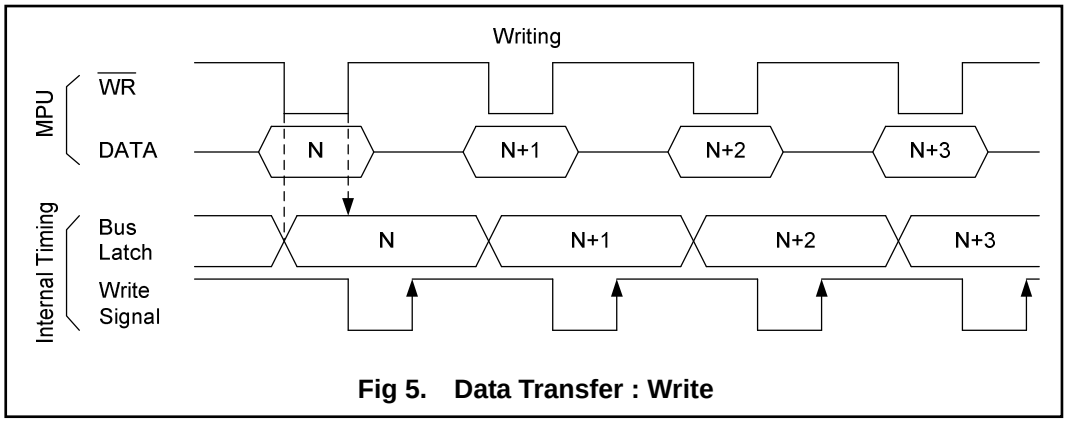


Fig 5. Data Transfer : Write

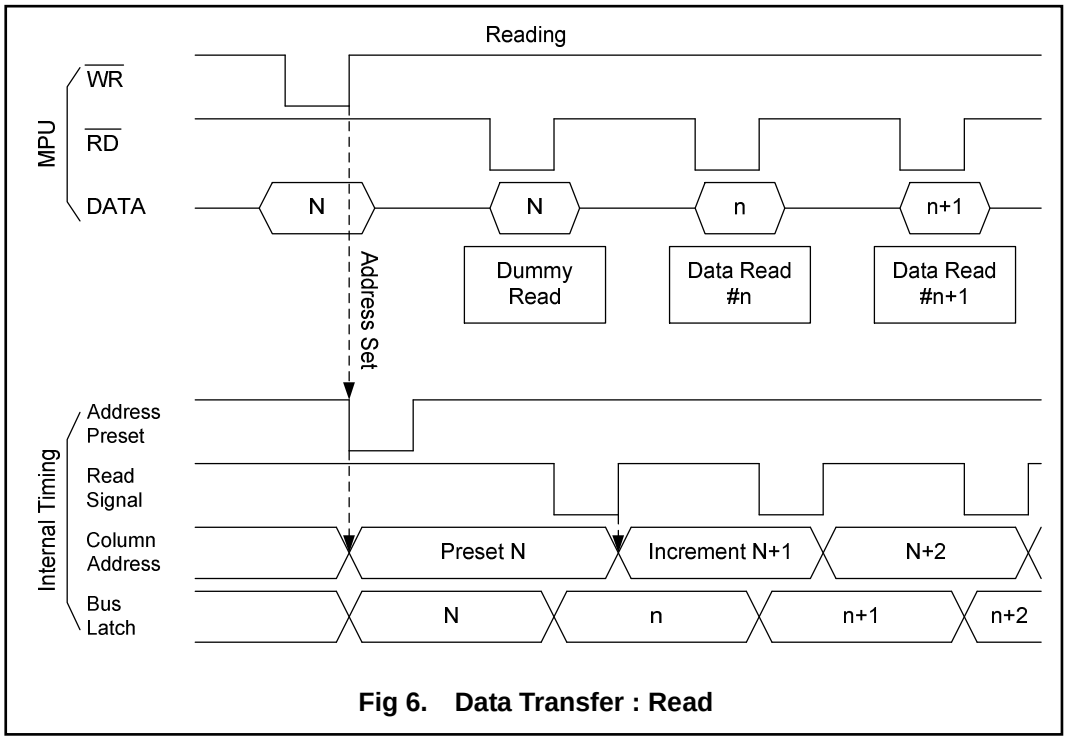


Fig 6. Data Transfer : Read

Display Data RAM (DDRAM)

ST7565P is built-in a RAM with 65X132 bit capacity which stores the display data. The display data RAM (DDRAM) store the dot data of the LCD. It is an addressable array with 132 columns by 65 rows (8-page with 8-bit and 1-page with 1-bit). The X-address is directly related to the column output number. Each pixel can be selected when the page and column addresses are specified (please refer to Fig 7 for detailed illustration). The rows are divided into: 8 pages (Page-0 ~ Page-7) each with 8 lines (for COM0~63) and Page-8 with only 1 line (COMS, for icon). The display data (D7~D0) corresponds to the LCD common-line direction and D0 is on top. All pages can be accessed through D[7:0] directly except icon page. Icon RAM uses only 1-bit of data bus (D0). Refer to Fig 8 for detailed illustration. The microprocessor can write to and read from (only Parallel interfaces) DDRAM by the I/O buffer. Since the LCD controller operates independently, data can be written into DDRAM at the same time as data is being displayed without causing the LCD flicker or data-conflict.

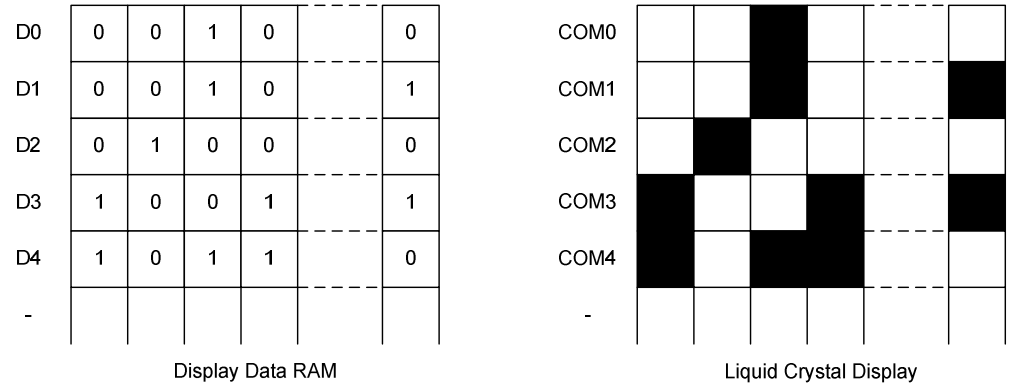


Fig 7. DDRAM Mapping Mode (Default Setting)

Fig 8. DDRAM Format

Addressing

Data is downloaded into the Display Data RAM matrix in ST7565P as byte-format. The Display Data RAM has a matrix of 65 by 132 bits. The address ranges are: X=0~131 (column address), Y=0~8 (page address). Addresses outside these ranges are not allowed.

Page Address Circuit

This circuit provides the page address of DDRAM. It incorporates 4-bit Page Address Register which can be modified by the “Page Address Set” instruction only. The Page Address must be set before accessing DDRAM content. Page Address “8” is a special RAM area for the icons with only one valid bit: D0.

Column Address Circuit

The column address of DDRAM is specified by the Column Address Set command. The column address is increased (+1) after each display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “83h”) because the Column Address and Page Address circuits are independent. For example, both Page Address and Column Address should be assigned for changing the DDRAM pointer from (Page-0, Column-83h) to (Page-1, Column-0).

Furthermore, Register MX and MY makes it possible to invert the relationship between the DDRAM and the outputs (COM/SEG). It is necessary to rewrite the display data into DDRAM after changing MX setting.

The relation between DDRAM and outputs with different MX or MY setting is shown below.

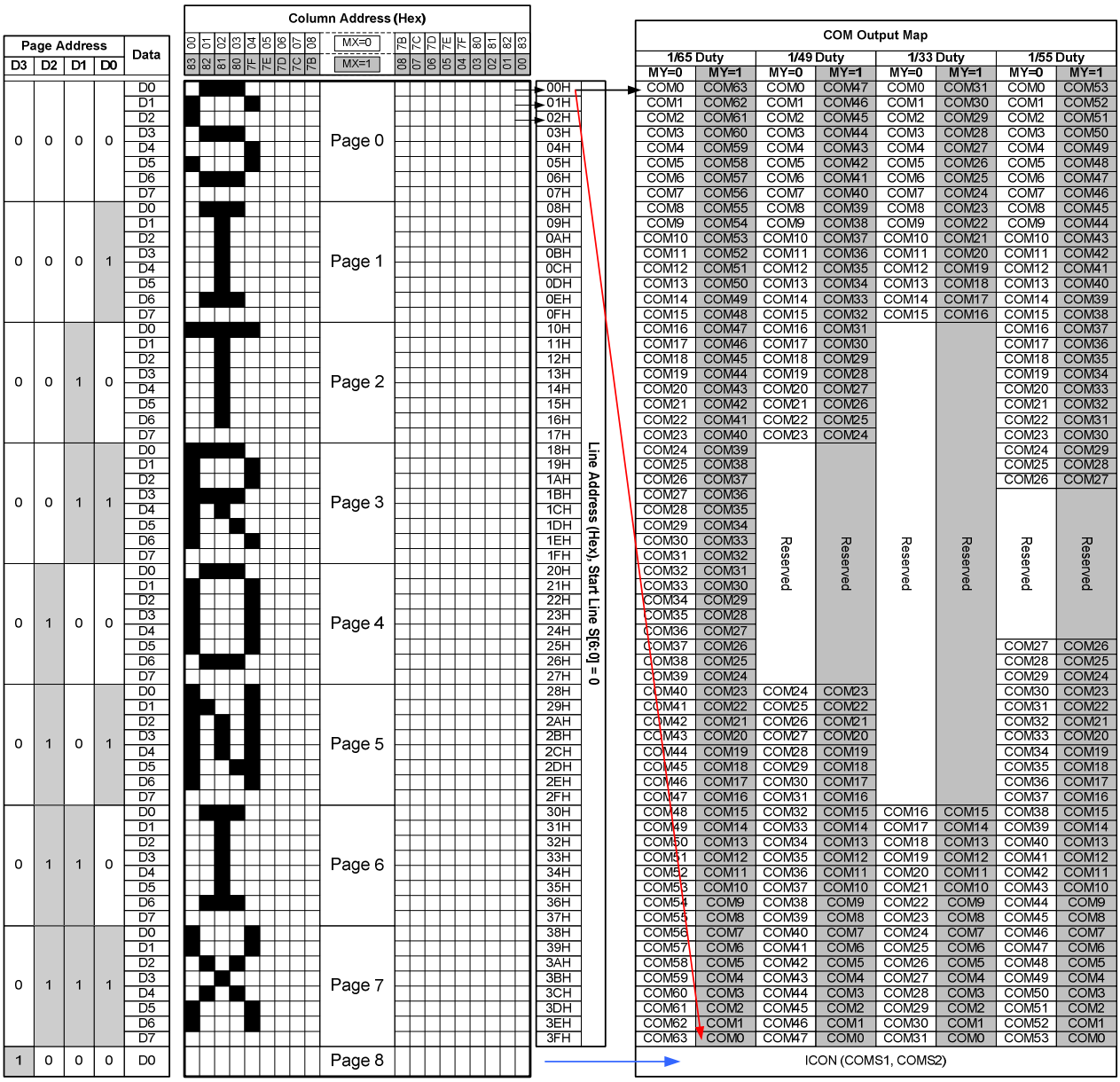


Fig 9. DDRAM and Output Map (COM/SEG)

Line Address Circuit

The Line Address Circuit incorporates a counter and a Line Address register which is changed only by the “Display Start Line Set” instruction. This circuit assigns DDRAM a Line Address corresponding to the first display line (COM0). Therefore, by setting Line Address repeatedly, ST7565P can realize the screen scrolling without changing the contents of DDRAM as shown in Fig 10. The last common is always the COMS (common output for the icons). That means the icons will never scroll with the general display data.

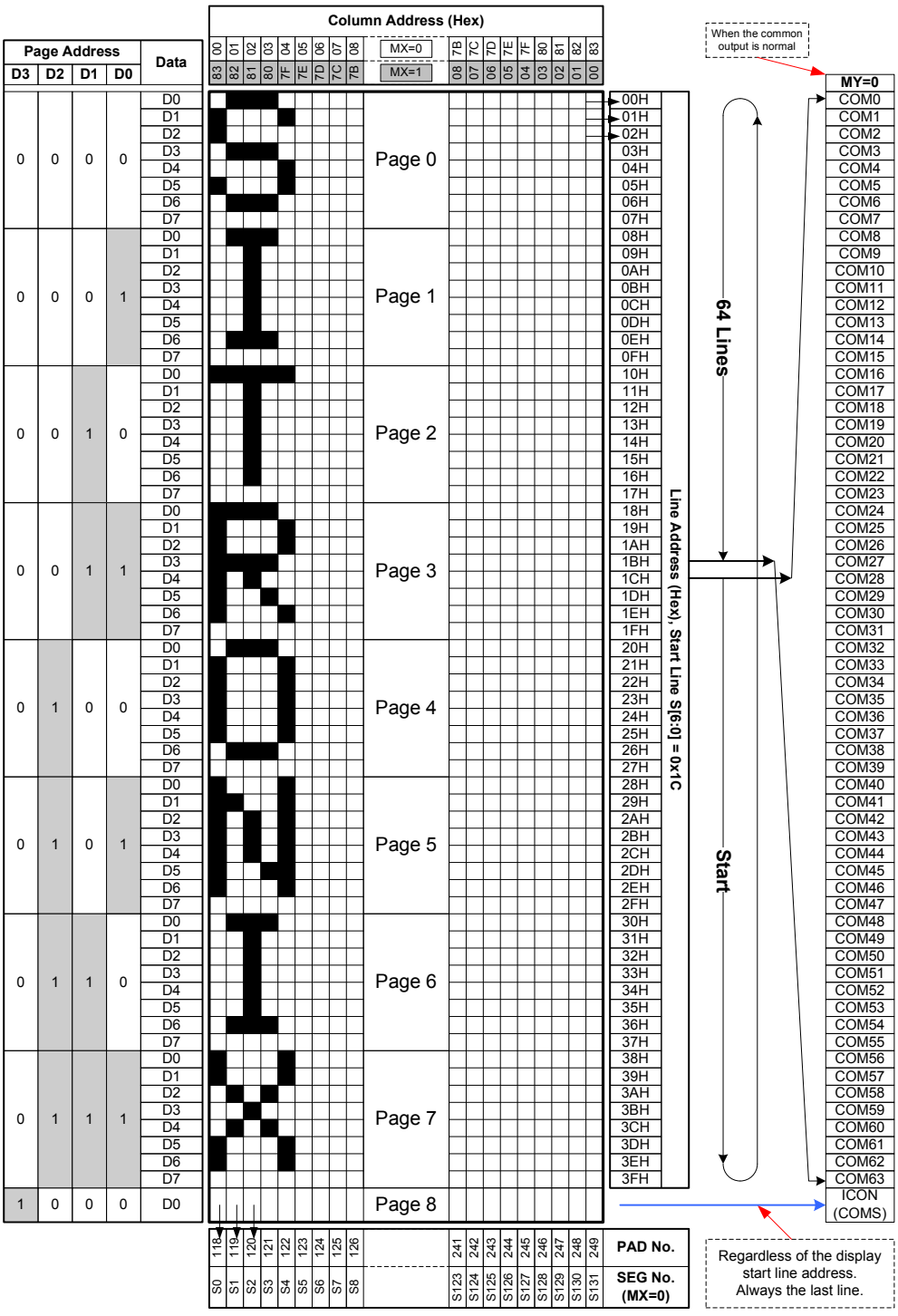


Fig 10. Start Line Function

Display Data Latch Circuit

The display data latch circuit latches temporarily display data of each segment output which will be output at the next clock. The special functions such as reverse display, display OFF and display all points ON only change the data in the latch and the content in the Display Data RAM is not changed.

Oscillation Circuit

The built-in oscillation circuit generates the system clock for the liquid crystal driving circuit. The oscillation circuit is enabled after initializing ST7565P. The clock will not be output to reduce the power consumption.

Liquid Crystal Driver Power Circuit

The built-in power circuits generate the voltage levels which are necessary to drive the liquid crystal. The built-in power system has voltage booster, voltage regulator and voltage follower circuits. The functionality of voltage booster, voltage regulator and voltage follower circuits can be turned ON and OFF individually. ST7565P is possible to use built-in power circuit and external power supply through the command “Power Control Set”. The relationship of command setting and power using is shown below. Before power ST7565P OFF, a Power OFF procedure is needed (please refer to the OPERATION FLOW section).

Power Control Set			Built-in Circuit			Power Supply					
VB	VR	VF	Booster	Regulator	Follower	VOUT	V0	V1	V2	V3	V4
1	1	1	ON	ON	ON	Internal	Internal	Internal	Internal	Internal	Internal
0	1	1	OFF	ON	ON	External	Internal	Internal	Internal	Internal	Internal
0	0	1	OFF	OFF	ON	External	External	Internal	Internal	Internal	Internal
0	0	0	OFF	OFF	OFF	External	External	External	External	External	External

Table 4. Power Control

Booster Circuit

Base on VDD2-VSS, ST7565P is able to product step-up voltages of x2, x3, x4, x5 and x6 through hardware and software setting.

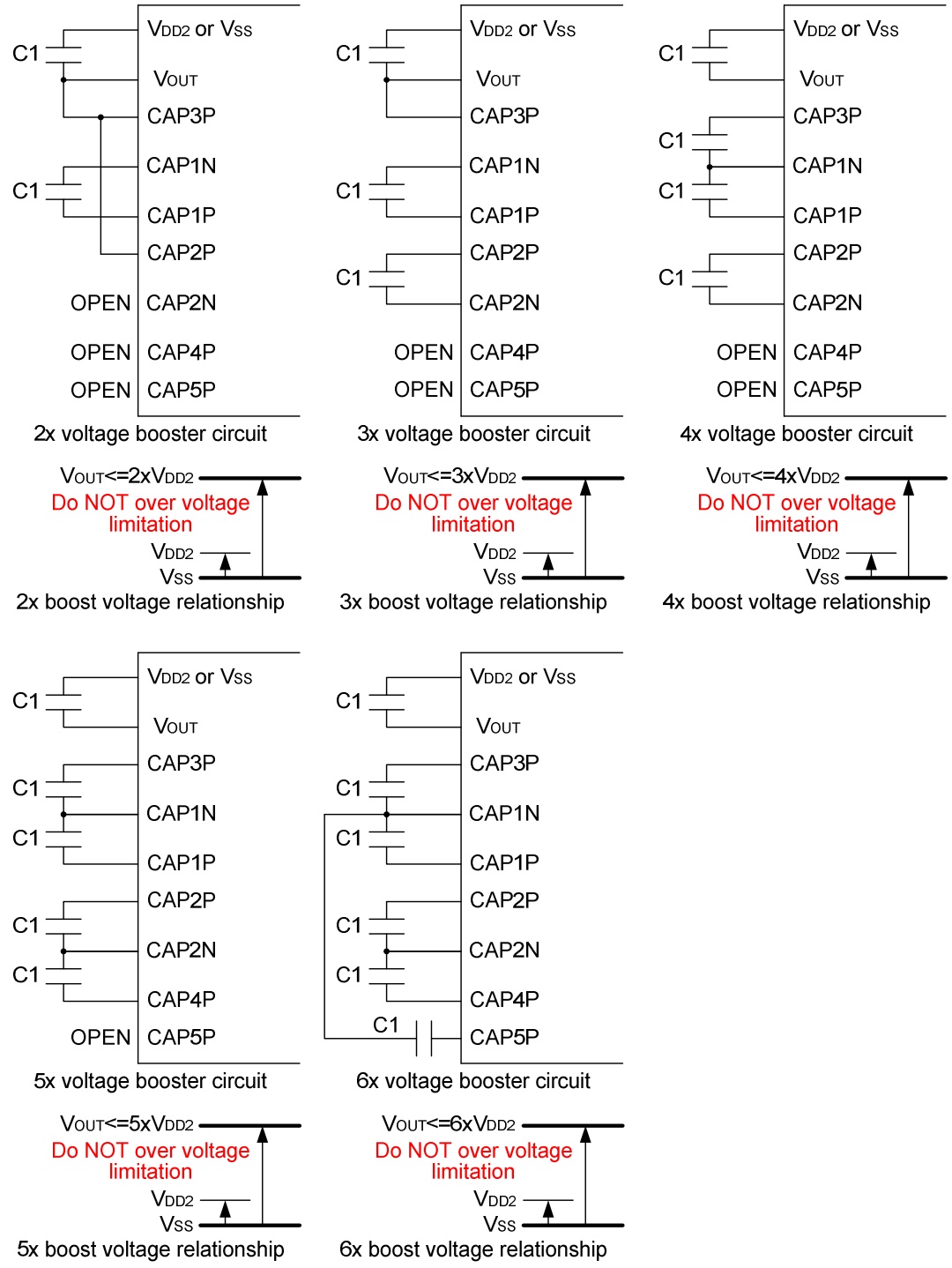


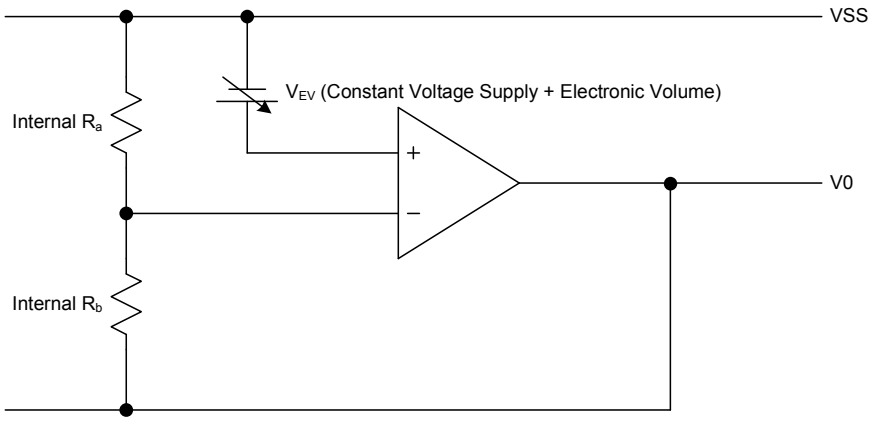
Fig 11. External Component of Booster Circuit

Regulator Circuit

ST7565P provides two kinds power supply for LCD driving voltage V0. Built-in regulator circuit or external power supply for V0 is available for LCD driving. The built-in high accuracy regulation circuit has 8 regulation ratios and each one has 64 EV-levels for voltage adjustment. Without additional external component, the output voltage can be changed by instructions such as “Regulation Ratio” and “Set EV”. The detailed setting method can be found in the INSTRUCTION DESCRIPTION section.

Built-in Resistor Is Used For Regulator Circuit

The internal regulator circuit can be controlled by built-in regulation ratio and the electronic volume setting.



$$V0 = \left(1 + \frac{R_b}{R_a}\right) \times V_{EV}$$

$$= \left(1 + \frac{R_b}{R_a}\right) \times \left(1 - \frac{\alpha}{162}\right) \times V_{REG}$$

$$V_{EV} = \left(1 - \frac{\alpha}{162}\right) \times V_{REG}$$

Fig 12. Built-in Regulation Ratio

V_{REG} is built-in constant voltage supply for regulator circuit. The voltage level of V_{REG} is 2.1V at temperature 25℃. α is determined by command “Set EV”. Base on command “Set EV”, the relationship between EV[5:0] and α is shown below.

EV5	EV4	EV3	EV2	EV1	EV0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
0	0	0	0	1	1	60
:	:	:	:	:	:	:
1	1	1	1	0	0	3
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Table 5. Relationship between Electronic Volume and α

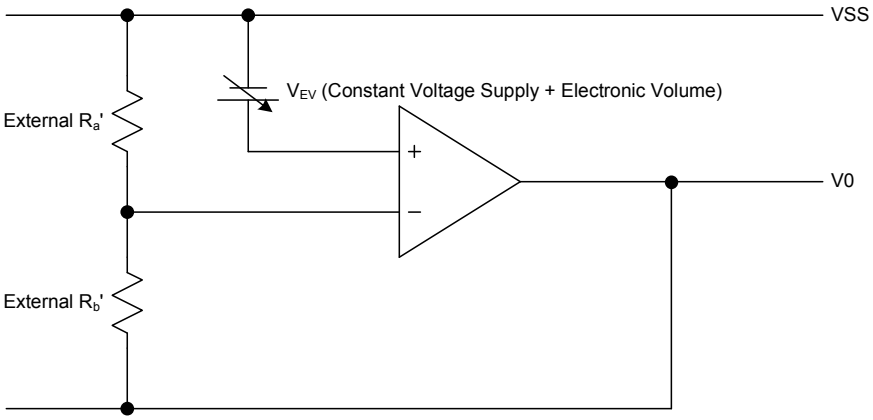
($1+R_b/R_a$) is internal regulation ratio for regulator circuit. The relationship between regulation ratio and RR[2:0] is shown below.

RR2	RR1	RR0	$1+R_b/R_a$
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

Table 6. Relationship between Regulation Ratio and RR[2:0]

External Resistor Is Used For Regulator Circuit

Through hardware setting IRS="L" and external resistor, ST7565P is able to use external regulation ratio to control the voltage level of V0.



$$V0 = \left(1+\frac{R_b'}{R_a'}\right) \times V_{EV}$$

$$= \left(1+\frac{R_b'}{R_a'}\right) \times \left(1-\frac{\alpha}{162}\right) \times V_{REG}$$

$$V_{EV} = \left(1-\frac{\alpha}{162}\right) \times V_{REG}$$

Fig 13. External Regulation Ratio

The setting condition of ST7565P for external regulation ratio is V0=8.0V, α=31 and V_{REG}=2.1V. The current consumption through R_a' and R_b' is limited to 5uA. Base on above condition, the relationship of R_a' and R_b' is $R_a' + R_b' = 1.6M\Omega$.

$$V0 = \left(1+\frac{R_b'}{R_a'}\right) \times \left(1-\frac{\alpha}{162}\right) \times V_{REG} \qquad (1.1)$$

$$8V = \left(1+\frac{R_b'}{R_a'}\right) \times \left(1-\frac{31}{162}\right) \times 2.1 \qquad (1.2)$$

$$R_a' + R_b' = 1.6M\Omega \qquad (1.3)$$

According to equation (1.2) and (1.3)

$$\frac{R_b'}{R_a'} = 3.71$$

$$R_a' = 340k\Omega$$

$$R_b' = 1260k\Omega$$

High Power Mode

ST7565P has two kinds of power mode for driving LCD. When HPMB pin is connected to “H” by VDD, ST7565P will enter normal power mode. Normal power mode has lower power consumption for driving. If the panel loading or size is larger, normal power mode may cause display quality to reduce. For improve display quality, ST7565P provides high power mode through connect HPMB pin to “L” by VSS.

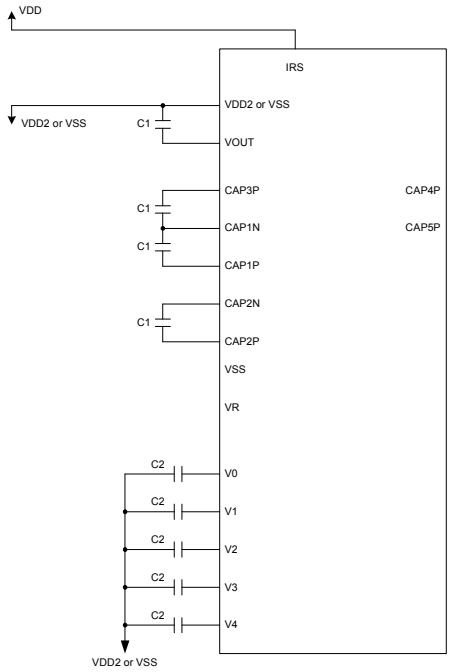
SITRONIX recommends that whether using high power mode or normal power mode is determined by actually display quality. Besides, if improvement is unsatisfactory after using high power mode, external power supply for LCD driving is necessary.

Power System Set

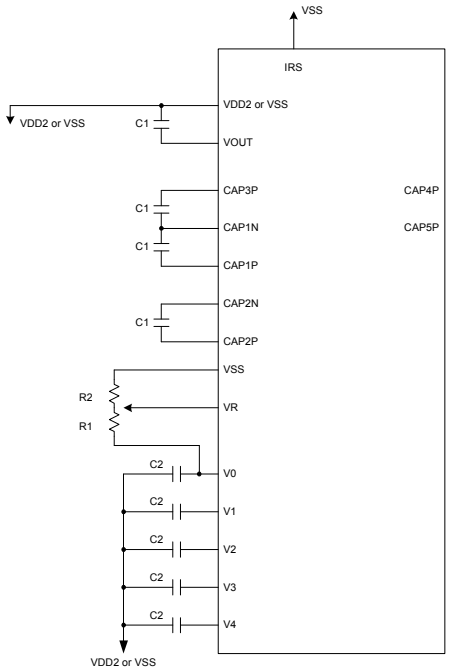
The following sections illustrate the connection of typical application.

Built-in Booster, Regulator and Follower Circuit are used

1. Built-in regulation ratio is used with x4 step-up

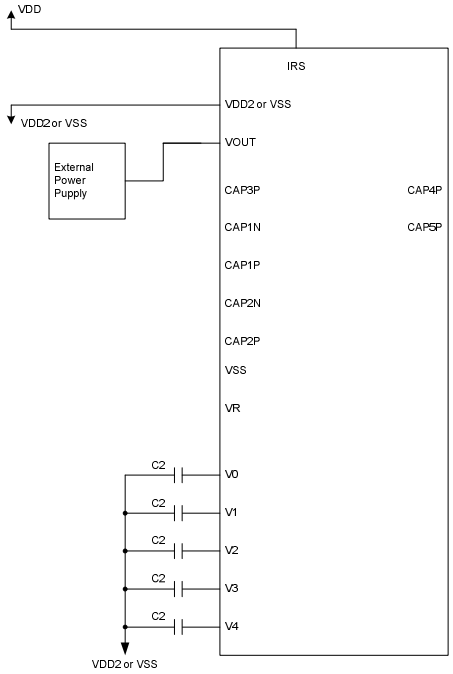


2. Built-in regulation ratio is not used with x4 step-up

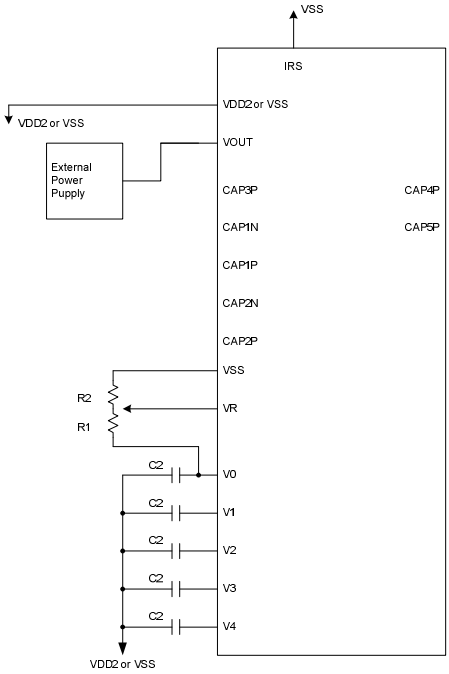


Built-in Regulator and Follower Circuit are alone used

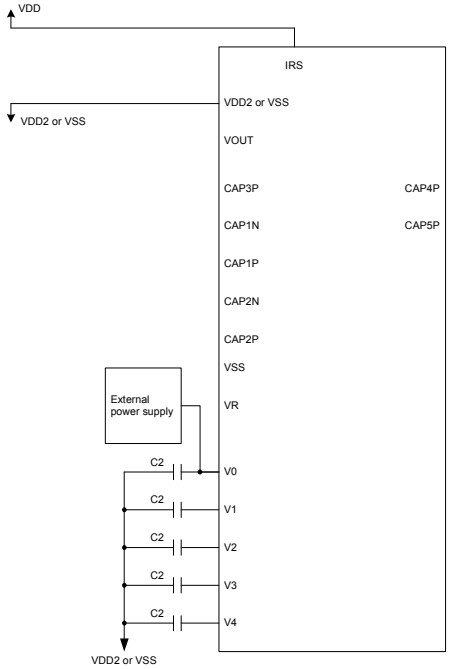
1. Built-in regulation ratio is used



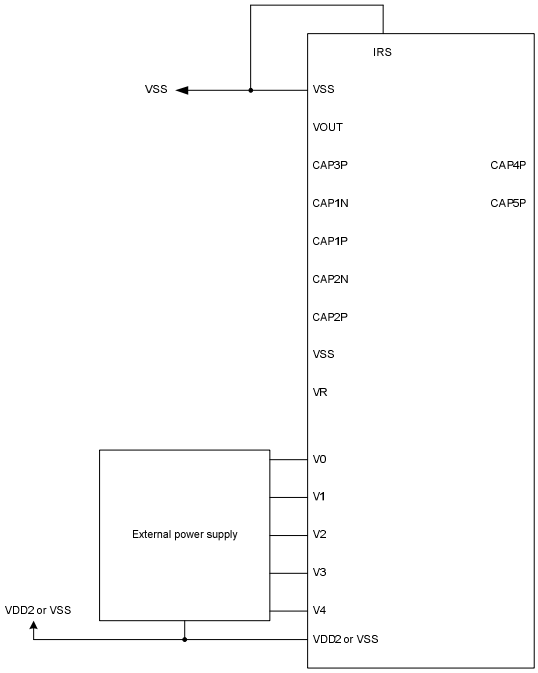
2. Built-in regulation ratio is not used



Built-in Follower Circuit is alone used



Built-in Booster, Regulator and Follower Circuit are not used



The optimum values of C1 and C2 are determined by panel loading and actually display quality. The values of capacitor should be determined by user. User should check display quality of used pattern and power stability after capacitor value is determined. The following table is a quick reference for the initial setting.

Symbol	Type	Reference Value (uF)
C1	Capacitor for step-up and LCD voltage stabilization	1.0 ~ 4.7
C2	Capacitor for LCD voltage stabilization	0.1 ~ 4.7

RESET CIRCUIT

Setting RSTB to “L” can initialize internal function. While RSTB is “L”, no instruction except read status can be accepted. RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating. Please note the hardware reset is not same as the software reset. When RSTB becomes “L”, the hardware reset procedure will start. When RESET instruction is executed, the software reset procedure will start. The procedure is listed below:

Procedure	Hardware Reset	Software Reset
Display OFF: D=0, all SEGs/COMs output at VSS	V	X
Normal Display: INV=0, AP=0	V	X
SEG Normal Direction: MX=0	V	X
Clear Serial Counter and Shift Register (if using Serial Interface)	V	X
Bias Selection: BS=0	V	X
Booster Level BL=0	V	X
Exit Power Saving Mode	V	X
Power Control OFF: VB=0, VR=0, VF=0	V	X
Exit Read-modify-Write mode	V	V
Static Indicator OFF	V	V
Static Indicator Register SIR[1:0]=(0,0)	V	V
Start Line S[5:0]=0	V	V
Column Address X[7:0]=0	V	V
Page Address Y[3:0]=0	V	V
COM Normal Direction: MY=0	V	V
V0 Regulation Ratio RR[2:0]=(1,0,0)	V	V
EV[5:0]=(1,0,0,0,0,0)	V	V
Exit Test Mode	V	V

After power-on, RAM data are undefined and the display status is “Display OFF”. It’s better to initialize whole DDRAM (ex: fill all 00h or write the display pattern) before turning the Display ON. Besides, the power is not stable at the time that the power is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

INSTRUCTION TABLE

INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	0	1	0	1	0	1	1	1	D	D=1, display ON D=0, display OFF
Set Start Line	0	0	0	1	S5	S4	S3	S2	S1	S0	Set display start line
Set Page Address	0	0	1	0	1	1	Y3	Y2	Y1	Y0	Set page address
Set Column Address	0	0	0	0	0	1	X7	X6	X5	X4	Set column address (MSB)
	0	0	0	0	0	0	X3	X2	X1	X0	Set column address (LSB)
Read Status	0	1	BUSY	MX	D	RST	0	0	0	0	Read IC Status
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write display data to RAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read display data from RAM
SEG Direction	0	0	1	0	1	0	0	0	0	MX	Set scan direction of SEG MX=1, reverse direction MX=0, normal direction
Inverse Display	0	0	1	0	1	0	0	1	1	INV	INV =1, inverse display INV =0, normal display
All Pixel ON	0	0	1	0	1	0	0	1	0	AP	AP=1, set all pixel ON AP=0, normal display
Bias Select	0	0	1	0	1	0	0	0	1	BS	Select bias setting 0=1/9; 1=1/7 (at 1/65 duty)
Read-modify-Write	0	0	1	1	1	0	0	0	0	0	Column address increment: Read:+0 , Write:+1
END	0	0	1	1	1	0	1	1	1	0	Exit Read-modify-Write mode
RESET	0	0	1	1	1	0	0	0	1	0	Software reset
COM Direction	0	0	1	1	0	0	MY	-	-	-	Set output direction of COM MY=1, reverse direction MY=0, normal direction
Power Control	0	0	0	0	1	0	1	VB	VR	VF	Control built-in power circuit ON/OFF
Regulation Ratio	0	0	0	0	1	0	0	RR2	RR1	RR0	Select regulation resistor ratio
Set EV	0	0	1	0	0	0	0	0	0	1	Double command!! Set electronic volume (EV) level
	0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0	
Power Save	0	0	Compound Command								Display OFF + All Pixel ON
Set Booster	0	0	1	1	1	1	1	0	0	0	Double command!! Set booster level: BL[1:0]=(0,0), x2, x3, x4 BL[1:0]=(0,1), x5 BL[1:0]=(1,1), x6
	0	0	0	0	0	0	0	0	BL1	BL0	
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Test	0	0	1	1	1	1	-	-	-	-	Do NOT use. Reserved for testing.

Note: Symbol “-” means this bit can be “H” or “L”.

INSTRUCTION DESCRIPTION

Display ON/OFF

The D flag selects the display mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	1	1	1	D

D=1: Normal Display Mode.

D=0: Display OFF. All SEGs/COMs output with VSS.

Set Start Line

This instruction sets the line address of the Display Data RAM to determine the initial display line. The display data of the specified line address is displayed at the top row (COM0) of the LCD panel.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	S5	S4	S3	S2	S1	S0

S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
0	0	0	0	1	1	3
:	:	:	:	:	:	:
1	1	1	1	0	1	61
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Page Address

Y [3:0] defines the Y address vector address of the display RAM.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	1	Y3	Y2	Y1	Y0

Y3	Y2	Y1	Y0	Page Address	Valid Bit
0	0	0	0	Page0	D0~ D7
0	0	0	1	Page1	D0~ D7
0	0	1	0	Page2	D0~ D7
:	:	:	:	:	:
0	1	1	0	Page6	D0~ D7
0	1	1	1	Page7	D0~ D7
1	0	0	0	Page8 (icon page)	D0

Set Column Address

The range of column address is 0…131. The parameter is separated into 2 instructions. The column address is increased (+1) after each byte of display data access (read/write). This allows MPU accessing DDRAM content continuously. This feature stops at the end of each page (Column Address “83h”).

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	X7	X6	X5	X4

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	X3	X2	X1	X0

X7	X6	X5	X4	X3	X2	X1	X0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	120
1	0	0	0	0	0	1	1	131

Read Status

Read the internal status of ST7565P. The read function is not available in serial interface mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	BUSY	MX	D	RST	0	0	0	0

Flag	Description
BUSY	BUSY=0: Command can be accepted BUSY=1: Command or reset procedure is executed
MX	MX=0: Reverse direction (SEG131->SEG0) MX=1: Normal direction (SEG0->SEG131)
D	D=0: Display ON D=1: Display OFF
RST	RST=1: During reset (hardware or software reset) RST=0: Normal operation

Write Data

8-bit data of Display Data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page. During auto-increment, the column address wraps to 0 after the last column is written.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	Write Data							

Read Data

8-bit data of Display Data from the RAM location specified by the column address and page address can be read to the microprocessor. The read function is not available in serial interface mode.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

SEG Direction

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	0	MX

Flag	Description
MX	MX=0: Normal direction (SEG0->SEG131) MX=1: Reverse direction (SEG131->SEG0)

Inverse Display

This instruction changes the selected and non-selected voltage of SEG. The display will be inversed (white -> Black, Black -> White) while the display data in the Display Data RAM is never changed.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	1	INV

Flag	Description
INV	INV=0: Normal display INV =1: Inverse display

All Pixel ON

This instruction will let all segments output the selected voltage and make all pixels turned ON.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	1	0	AP

Flag	Description
AP	AP =0: Normal display AP =1: All pixels ON

Bias Select

Select LCD bias ratio of the voltage required for driving the LCD.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	1	0	0	0	1	BS

Duty	Bias	
	BS=0	BS=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6
1/53	1/8	1/6

Reference LCD Bias Voltage (1/65 Duty with 1/9 Bias)

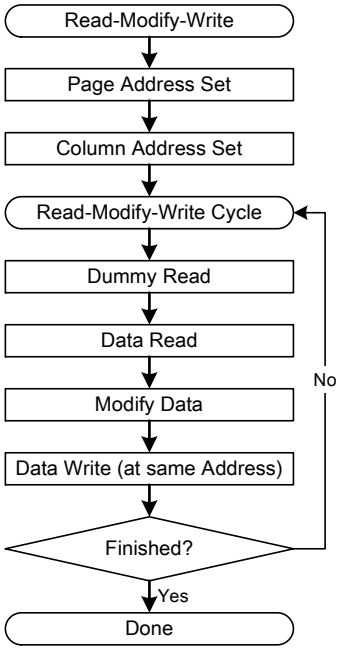
Symbol	Bias Voltage
V0	V0
V1	8/9 x V0
V2	7/9 x V0
V3	2/9 x V0
V4	1/9 x V0
VSS	VSS

Read-modify-Write

This command is used paired with the “END” instruction. Once this command has been input, the display data read operation will not change the column address, but only the display data write operation will increase the column address (X[7:0]+1). This mode is maintained until the END command is input. This function makes it possible to reduce the load on the MPU when there are repeating data changes in a specified display region, such as a blanking cursor.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	0	0

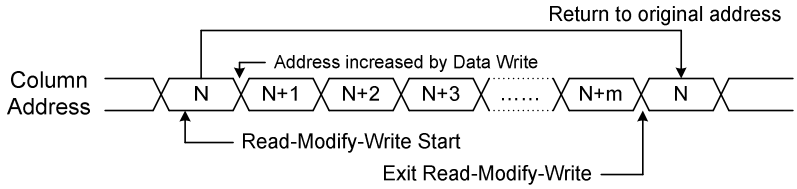
* In Read-modify-Write mode, other instructions aside from display data read/write commands can also be used.



END

When the END command is input, the Read-modify-Write mode is released and the column address returns to the address it was when the Read-modify-Write instruction was entered.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	1	1	1	0



RESET

This instruction resets Start Line (S[5:0]), Column Address (X[7:0]), Page Address (Y[3:0]) and COM Direction (MY) to their default setting. Please note this instruction is not complete same as hardware reset (RSTB=L) and cannot initialize the built-in power circuit which is initialized by the RSTB pin. The detailed information is in “Section RESET CIRCUIT”.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	0

COM Direction

This instruction controls the common output status which changes the vertical display direction. The detailed information can be found in Fig 9.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	MY	-	-	-

Flag	Description
MY	MY=0: Normal direction (COM0->COM63) MY=1: Reverse direction (COM63->COM0)

Power Control

This instruction controls the built-in power circuits. Typically, these 3 flags are turned ON at the same time.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	1	VB	VR	VF

Flag	Description
VB	VB=0: Built-in Booster OFF VB=1: Built-in Booster ON
VR	VR=0: Built-in Regulator OFF VR=1: Built-in Regulator ON
VF	VF=0: Built-in Follower OFF VF=1: Built-in Follower ON

Regulation Ratio

This instruction controls the regulation ratio of the built-in regulator.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	RR2	RR1	RR0

RR2	RR1	RR0	Regulation Ratio (RR)
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0
1	0	1	5.5
1	1	0	6.0
1	1	1	6.5

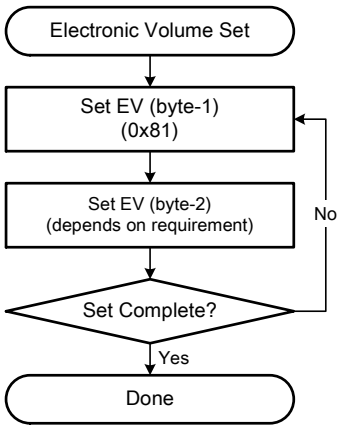
The operation voltage (V0) calculation formula is shown below: (RR comes from Regulation Ratio, EV comes from EV[5:0])
V0 = RR X [1 – (63 – EV) / 162] X 2.1, or **V0 = RR X [(99 + EV) / 162] X 2.1**

SYMBOL	REGISTER	VALUE
RR	RR[2:0]	3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0 and 6.5
EV	EV[5:0]	0~63

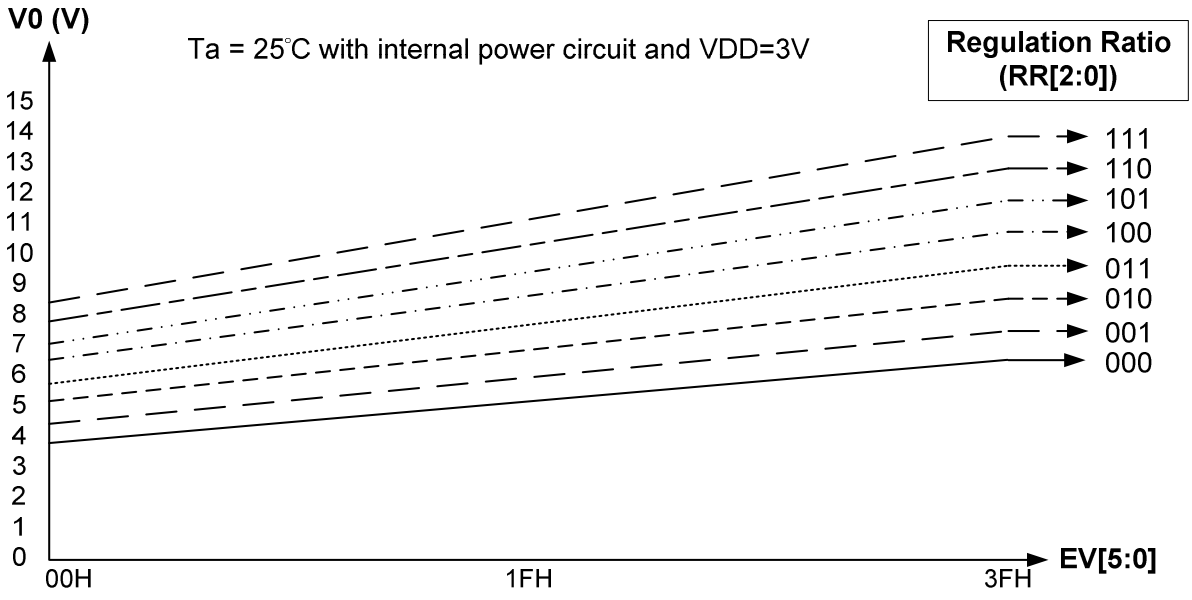
Set EV

This is double byte instruction. The first byte set ST7565P into EV adjust mode and the following instruction will change the EV setting. That means these 2 bytes must be used together. They control the electronic volume to adjust a suitable V0 voltage for the LCD.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0	0	1
0	0	0	0	EV5	EV4	EV3	EV2	EV1	EV0



The maximum voltage that can be generated is dependent on the VDD2 voltage and the loading of LCD module. There are 8 V0 voltage curve can be selected. It is recommended the EV should be close to the center (1FH) for easy contrast adjustment. Please refer to the “Selection of Application Voltage” section for detailed information.



EV[5:0] and RR[2:0] vs. V0 Voltage

Fig 21 Setting V0 Voltage

Power Save (Compound Instruction)

This is compound instruction. The 1st instruction is Display OFF (D=0) and the 2nd instruction is All Pixel ON (AP=1). The Power Save mode starts the following procedure: (the display data and register settings are still kept except D-Flag and AP-Flag)

1. Stops internal oscillation circuit;
2. Stops the built-in power circuits;
3. Stops the LCD driving circuits and keeps the common and segment outputs at VSS.

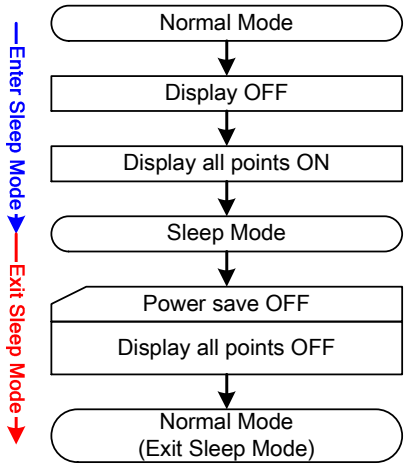


Fig 21 Power Save Procedure

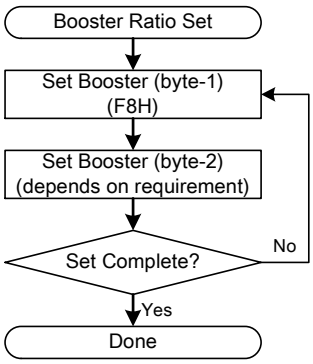
After exiting Power Save, the settings will return to be as they were before.

Set Booster

This is double byte instruction. The first byte set ST7565P into booster configuration mode and the following instruction will change the booster setting. That means these 2 bytes must be used together. They control the built-in booster circuit to provide the power source of the built-in regulator. Hardware connection should be changed according to booster level setting. If the hardware connection and software setting is not corresponding, ST7565P will cause extra power consumption. ST7565P will not damage through the extra power consumption.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	0	0	0
0	0	0	0	0	0	0	0	BL1	BL0

BL1	BL0	Boost Level
0	0	X2, x3, x4
0	1	x5
1	1	x6



NOP

“No Operation” instruction. ST7565P will do nothing when receiving this instruction.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	0	0	0	1	1

Test

The test mode is reserved for IC testing. Please don’t use this instruction. If the test mode is enabled accidentally, it can be cleared by: issuing an “L” pulse on RSTB pin, issuing RESET instruction or issuing NOP instruction.

A0	R/W(RWR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	-	-	-	-

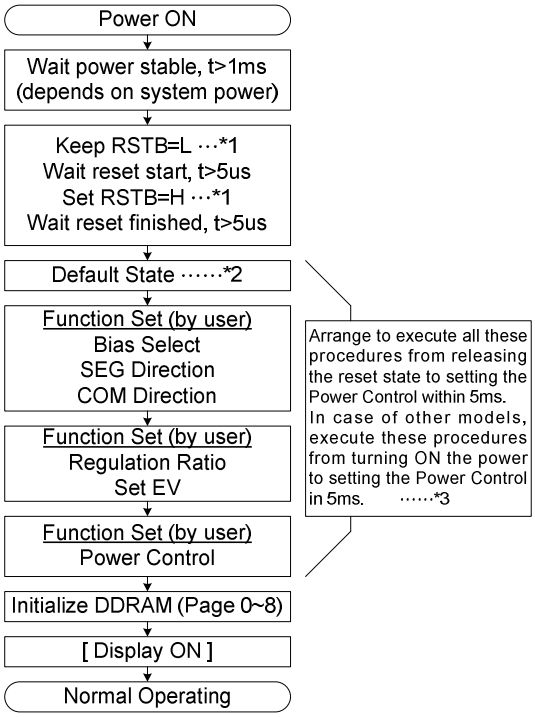
Note: “-” means “1” or “0”.

OPERATION FLOW

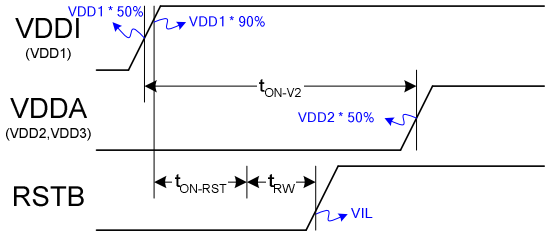
This section introduces some reference operation flows.

Power ON

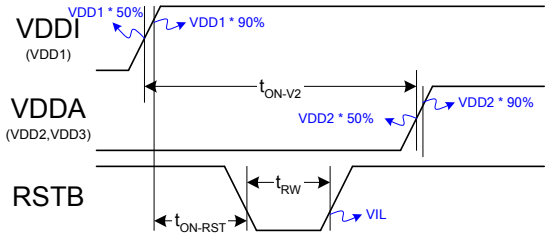
Referential Operation Flow	Operation Sequence



Case 1: RSTB=L while Power ON



Case 2: RSTB=H while Power ON



Note: The detailed description can be found in the respective sections listed below.

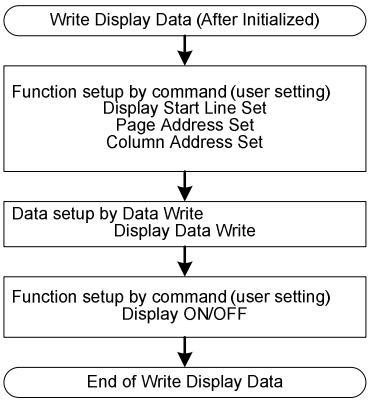
1. Please refer to the timing specification of t_{RW} and t_R.
2. Refer to Section RESET CIRCUIT.
3. The 5ms requirement depends on the characteristics of LCD panel and the external component of the power circuit. It is recommended to check with the real products with external component.
4. The detailed instruction functionality is described in Section INSTRUCTION DESCRIPTION;
5. Power stable is defined as the time that the later power (VDDI or VDDA) reaches 90% of its rated voltage.

Timing Requirement:

Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● Applying VDDI and VDDA in any order will not damage IC.
RSTB input time	t_{ON-RST}	No Limitation	● If RSTB is Low, High or unstable during power ON, a successful hardware reset by RSTB is required after VDDI is stable. ● RSTB=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RSTB. ● To prevent abnormal display, the recommended timing is: $0 \le t_{ON-RST} \le 30$ ms.

- The requirement listed here is to prevent abnormal display on LCD module.

Display Data

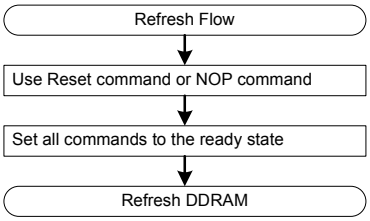


Notes: Reference items

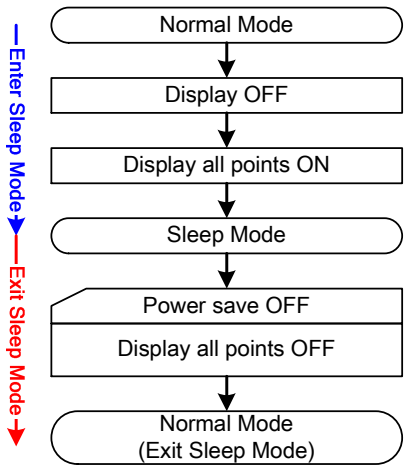
1. The detailed instruction functionality is described in Section INSTRUCTION DESCRIPTION;
2. It is recommended to write display data (initialize DDRAM) before Display ON.

Refresh

It is recommended to use the refresh sequence regularly in a specified interval.



Power-Save Flow and Sequence

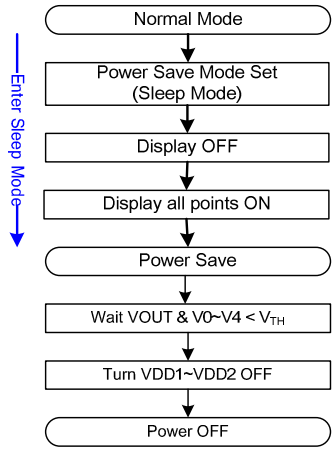


Power OFF Flow and Sequence

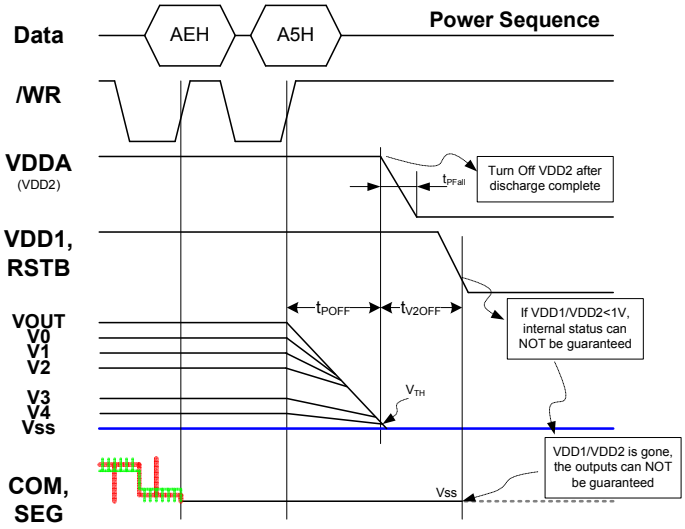
In power save mode, LCD outputs are fixed to VSS and all analog outputs are discharged. The power can be turned OFF after ST7565P is in the power save mode. The power save mode can be triggered by the following two methods.

Referential Power OFF Flow	*Operation Sequence*

CASE 1: Use Power Save Instruction



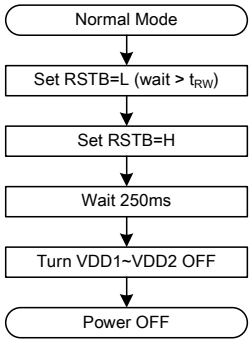
Power OFF Flow



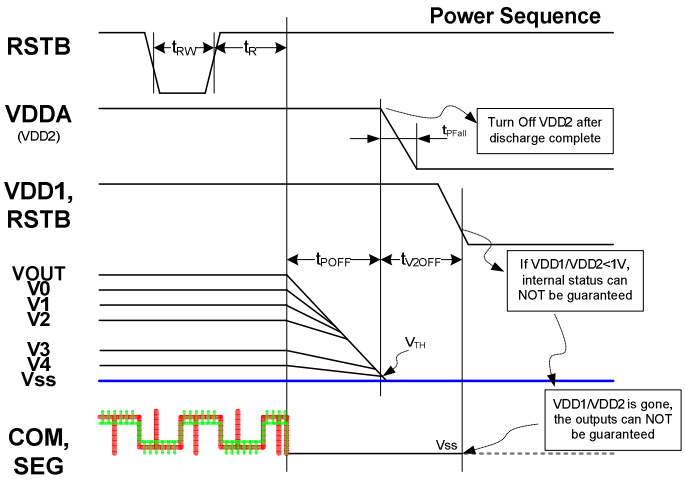
Instruction Flow

After the built-in power circuits are OFF and completely discharged (the power level of built-in analog circuit is smaller than V_{TH} of LCD panel), the power (VDDI, VDDA) can be removed. V_{TH} is around 0.2V to 1.0V.

CASE 2: Use Hardware Reset Function



Power OFF Flow



Instruction Flow

After the built-in power circuits are OFF and completely discharged (the power level of built-in analog circuit is smaller than V_{TH} of LCD panel), the power (VDDI, VDDA) can be removed. V_{TH} is around 0.2V to 1.0V.

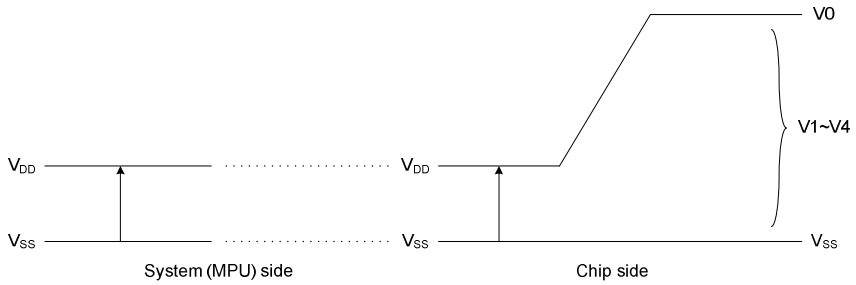
Note:

1. t_{POFF}: Internal Power discharge time. Discharge time for built-in circuit is dependent on user's system design.
2. t_{V2OFF}: Period between VDDI and VDDA OFF time. => 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.
4. IC will NOT be damaged if either VDDI or VDDA is OFF while another is ON.
5. The timing is dependent on panel loading and the external capacitor(s).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
Digital Power Supply Voltage	VDD	-0.3 ~ 3.6	V
Analog Power supply voltage	VDD2	-0.3 ~ 3.6	V
LCD Power supply voltage	VOUT, V0	-0.3 ~ 14.5	V
LCD Power supply voltage	V1, V2, V3, V4	-0.3 ~ V0	V
Operating temperature	TOPR	–30 to +80	°C
Storage temperature	TSTR	–55 to +125	°C



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure the voltage levels of VOUT, V0, V1, V2, V3, V4 and VSS always match the correct relation:
   VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

VSS=0V; Tamb = -30°C to +80°C; unless otherwise specified.

Item		Symbol	Condition		Rating			Unit	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD			1.8	—	3.3	V	VDD
Operating Voltage (2)		VDD2			2.4	—	3.3	V	VDD2
Input High-level Voltage		V_{IHC}			0.8 x VDD	—	VDD	V	MPU Interface
Input Low-level Voltage		V_{ILC}			VSS	—	0.2 x VDD	V	MPU Interface
Output High-level Voltage		V_{OHC}	I_{OUT}=1mA, VDD=1.8V		0.8 x VDD	—	VDD	V	D[7:0]
Output Low-level Voltage		V_{OLC}	I_{OUT}=-1mA, VDD=1.8V		VSS	—	0.2 x VDD	V	D[7:0]
Input Leakage Current		I_{LI}			−1.0	—	1.0	μA	MPU Interface
Output Leakage Current		I_{LO}			−3.0	—	3.0	μA	MPU Interface
Supply Voltage Follower Circuit		V_0			4.0	—	13.5	V	V0
Reference Voltage		V_{RS}	Ta=25°C		2.07	2.10	2.13	V	VRS
Liquid Crystal Driver ON Resistance		R_{ON}	Ta=25°C	V0=13V	—	2.0	3.5	KΩ	COMx
				V0=8V	—	3.2	5.4	KΩ	SEGx
Oscillator Frequency	Internal Oscillator	f_{OSC}	1/65 Duty 1/33 Duty	Ta=25°C	17	20	24	kHz	
	External Oscillator	f_{CL}			17	20	24	kHz	CL
	Internal Oscillator	f_{OSC}	1/49 Duty 1/53 Duty 1/55 Duty	Ta=25°C	25	30	35	kHz	
	External Oscillator	f_{CL}			25	30	35	kHz	CL

Current consumption: During Display, without internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW (Static)	ISS	VDD=VDD2 =3.0V, V0=11.0V, Ta=25°C	—	19	32	μA	
Display OFF	ISS	VDD=VDD2 =3.0V, V0=11.0V, Ta=25°C	—	16	27	uA	

Current consumption: During Display, with internal power system, current consumed by whole IC (bare die).

Test Pattern	Symbol	Condition	Rating			Unit	Note
			Min.	Typ.	Max.		
Display Pattern: SNOW	ISS	VDD=VDD2 =3.0V, V0=11.0V, Booster=x4, Ta=25°C	—	100	147	uA	Normal Mode
			—	135	205	uA	High Power Mode
Display OFF	ISS	VDD=VDD2 =3.0V, V0=11.0V, Booster=x4, Ta=25°C	—	90	130	uA	Normal Mode
			—	128	193	uA	High Power Mode
Sleep Mode	ISS	VDD=VDD2 =3.0V, Ta=25°C	—	0.1	4	uA	

Note:

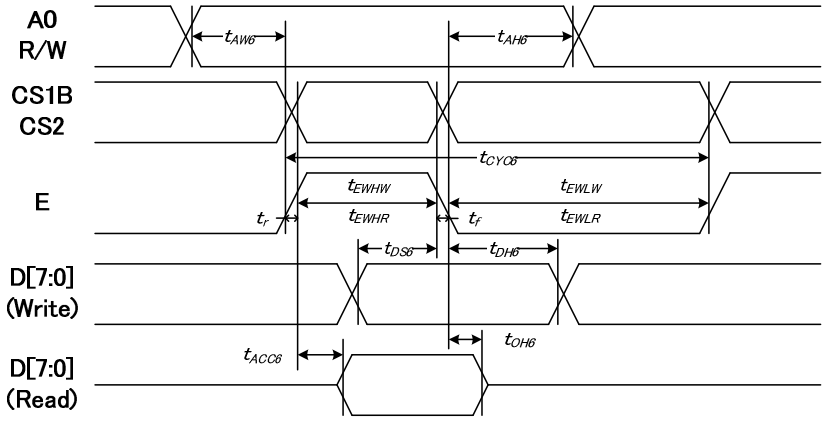
- *The Current Consumption is DC characteristics*

The relationship between oscillator frequency f_{OSC}, display clock frequency f_{CL} and liquid crystal frame rate frequency f_{FR}

Item		f_{CL}	f_{FR}
1/65 Duty	Internal Oscillator Circuit	fOSC / 4	fOSC / 4 / 65
	External Display Clock	External Display Clock (f_{CL})	f_{CL} / 260
1/49 Duty	Internal Oscillator Circuit	fOSC / 8	fOSC / 4 / 49
	External Display Clock	External Display Clock (f_{CL})	f_{CL} / 196
1/33 Duty	Internal Oscillator Circuit	fOSC / 8	fOSC / 4 / 33
	External Display Clock	External Display Clock (f_{CL})	f_{CL} / 264
1/55 Duty	Internal Oscillator Circuit	fOSC / 8	fOSC / 4 / 55
	External Display Clock	External Display Clock (f_{CL})	f_{CL} / 220
1/53 Duty	Internal Oscillator Circuit	fOSC / 8	fOSC / 4 / 53
	External Display Clock	External Display Clock (f_{CL})	f_{CL} / 212

TIMING CHARACTERISTICS

System Bus Timing for 6800 Series MPU



(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		240	—	
Enable L pulse width (WRITE)		tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)		tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		0	—	
Read data access time		tACC6	CL = 100 pF	—	70	
Read data output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		400	—	
Enable L pulse width (WRITE)		tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)		tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
Write data setup time	D[7:0]	tDS6		40	—	
Write data hold time		tDH6		0	—	
Read data access time		tACC6	CL = 100 pF	—	140	
Read data output disable time		tOH6	CL = 100 pF	10	100	

(VDD = 1.8V , Ta =25°C)

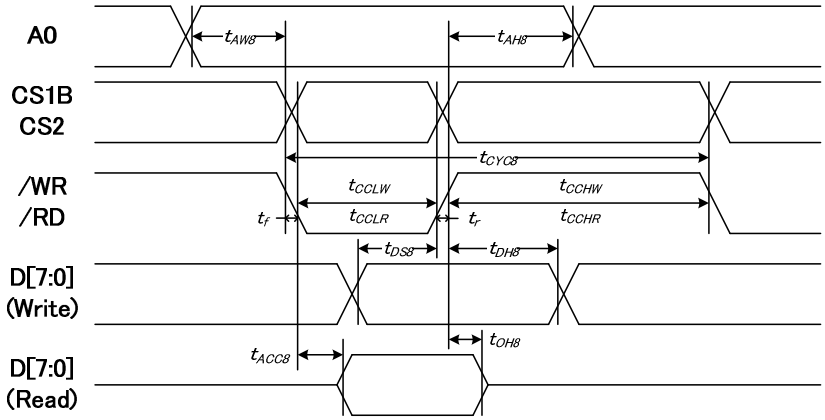
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		0	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		640	—	
Enable L pulse width (WRITE)		tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)		tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
Write data setup time	D[7:0]	tDS6		80	—	
Write data hold time		tDH6		0	—	
Read data access time		tACC6	CL = 100 pF	—	240	
Read data output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CS1B being “L” (CS2=“H”) and E.

System Bus Timing for 8080 Series MPU



(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		240	—	
/WR L pulse width (WRITE)		tCCLW		80	—	
/WR H pulse width (WRITE)		tCCHW		80	—	
/RD L pulse width (READ)	RD	tCCLR		140	—	
/RD H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		400	—	
/WR L pulse width (WRITE)		tCCLW		220	—	
/WR H pulse width (WRITE)		tCCHW		180	—	
/RD L pulse width (READ)	RD	tCCLR		220	—	
/RD H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D[7:0]	tDS8		40	—	
WRITE Data hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

(VDD = 1.8V , Ta =25°C)

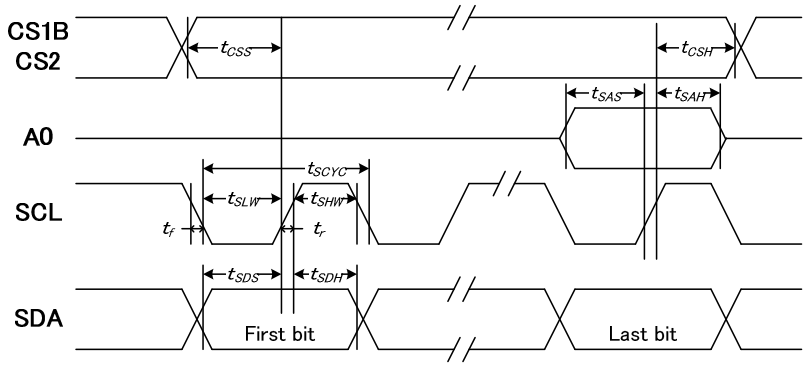
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		0	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		640	—	
/WR L pulse width (WRITE)		tCCLW		360	—	
/WR H pulse width (WRITE)		tCCHW		280	—	
/RD L pulse width (READ)	RD	tCCLR		360	—	
/RD H pulse width (READ)		tCCHR		280	—	
WRITE Data setup time	D[7:0]	tDS8		80	—	
WRITE Data hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between CS1B being “L” (CS2=“H”) and WR and RD being at the “L” level.

System Bus Timing for 4-Line Serial Interface



(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		50	—	ns
SCLK “H” pulse width		tSHW		25	—	
SCLK “L” pulse width		tSLW		25	—	
Address setup time	A0	tSAS		20	—	
Address hold time		tSAH		10	—	
Data setup time	SDA	tSDS		20	—	
Data hold time		tSDH		10	—	
CS-SCLK time	CS1B	tCSS		20	—	
CS-SCLK time	CS2	tCSH		40	—	

(VDD = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		100	—	ns
SCLK “H” pulse width		tSHW		50	—	
SCLK “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCLK time	CS1B	tCSS		30	—	
CS-SCLK time	CS2	tCSH		60	—	

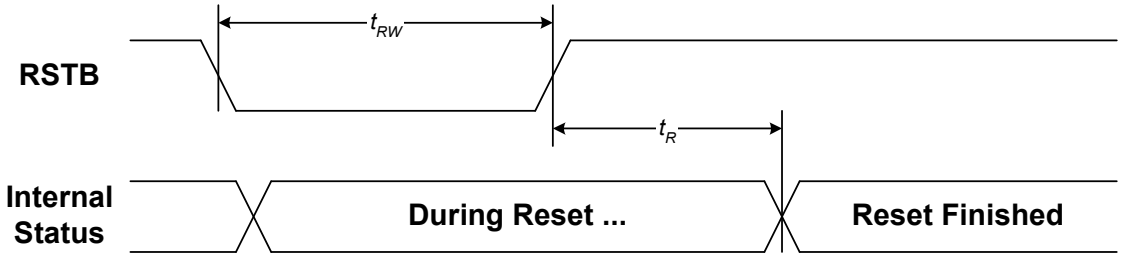
(VDD = 1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCLK	tSCYC		200	—	ns
SCLK “H” pulse width		tSHW		80	—	
SCLK “L” pulse width		tSLW		80	—	
Address setup time	A0	tSAS		60	—	
Address hold time		tSAH		30	—	
Data setup time	SDA	tSDS		60	—	
Data hold time		tSDH		30	—	
CS-SCLK time	CS1B	tCSS		40	—	
CS-SCLK time	CS2	tCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDD as the standard.

Hardware Reset Timing



(VDD = 3.3V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	1.0	us
Reset “L” pulse width	tRW		1.0	—	

(VDD = 2.7V , Ta =25°C)

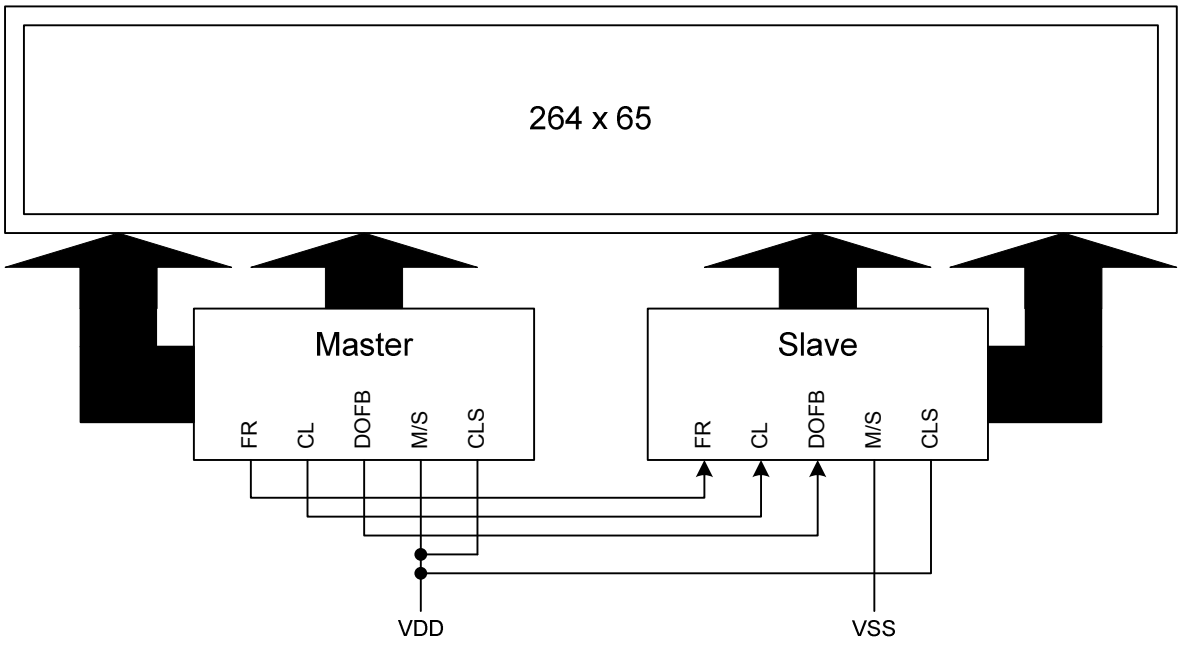
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2.0	us
Reset “L” pulse width	tRW		2.0	—	

(VDD = 1.8V , Ta =25°C)

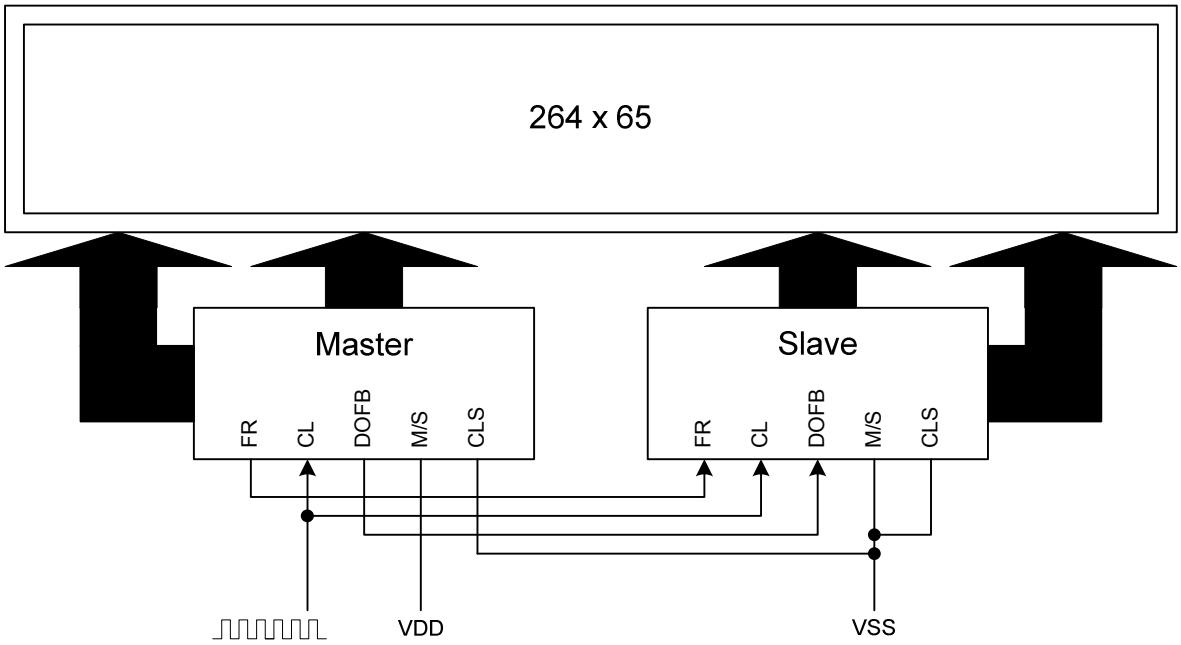
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	3.0	us
Reset “L” pulse width	tRW		3.0	—	

APPLICATION NOTE

Master/Slave Mode Using Internal Oscillator Circuit



Master/Slave Mode Using External Oscillator Clock



REVERSION HISTORY

Version	Date	Description
2004/04/05	Ver 1.2a	Modify Serial interface Timing Character.
2004/05/18	Ver 1.3	4. Change Temperature compensation rate to -0.05%/^{O}C.
2004/05/31	Ver 1.4	1. Add I/O pin ITO resistor limitation.
2004/06/24	Ver 1.5	Modify Page 2 PAD Diagram.
2004/07/14	Ver 1.6	Modify Page 19 V1~V4 voltage setting with different bias set command.
2005/09/22	Ver 1.7	● Modify Feature Description; ● Modify operating temperature; ● Modify PIN Name: PAD 80~85 to TEST0~5; ● Modify Absolute Maximum Ratings; ● Modify Ta of DC Characteristics and Reset Timing; ● Remove redundant Page 28; Modify reference voltage to Vss (Page 58, 59).
2006/02/13	Ver 1.8	● Modify the description of DC characteristics. ● Modify function description. ● Redraw figures. ● Redraw the PAD DIAGRAM. ● Highlight the HPM (High Power Mode) description. ● Put emphasis on the power OFF procedure (Page 56-57).
2006/03/10	Ver 1.9	● Fix Ver. 1.8: Booster Circuit mistake (Booster X6, Page 32).
2007/11/06	Ver 1.9a	● Modify PAD pitch between COM[40] and alignment mark of PAD DIAGRAM. (Page 2).
2008/02/19	Ver 1.9b	1. Modify Page 2 information: PAD 115, 290 and alignment mark drawing. ● Modify some description for easy understanding.
2008/03/14	Ver 1.9c	2. Modify Ver 1.9c mistake: alignment mark coordinate. 3. Add V_{IN} and V_O in Absolute Maximum Ratings. ● Modify description in Absolute Maximum Ratings.
2008/04/10	Ver 2.0	4. Remove Static Indicator function and command. 5. Reserved FRS pin function. 6. Truncated Alignment mark coordinate. 7. Rewrite some description. ● Update timing figures and naming.
2008/07/15	Ver 2.1	● Modify Page 2 information: bump size of PAD 115, 290.
2009/02/23	Ver 2.1a	● Modify mistake of Status Read.
2012/06/15	Ver 2.2	● Modify SPEC style ● Modify bump height